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13. ABSTRACT (Maximum 200 words)

Processing technologies for $Al_xGa_{1-x}N$ have been developed. Inductively-coupled-plasma reactive ion etching (ICP-RIE) is shown to be capable of etching AlGaN materials at high etch rates and high anisotropy. Plasma-induced damage in n-GaN is shown to depend mainly on the ion energy to which samples are exposed during ICP-RIE. The damage can be annealed at 700 °C with samples recovering to their unetched states. Photoelectrochemical etching of n-GaN is shown to be useful for material characterization and this process may be exploited as a rapid method for quantification of defects in GaN. Auger analysis and x-ray photoelectron spectroscopy have been utilized for studying the cleaning of $Al_xGa_{1-x}N$ surfaces; it is shown that buffered oxide etch is more effective in removing surface adventitious oxides of $Al_xGa_{1-x}N$ than ammonium hydroxide and hydrochloric acid. Schottky contacts on $Al_xGa_{1-x}N$ for various metals have been characterized. The barrier heights depend on metal workfunction which may show that $Al_xGa_{1-x}N$ surfaces are not completely dominated by surface states. Low contact ohmic resistances were achieved on p-GaN and p- $Al_xGa_{1-x}N$ /GaN superlattices using Ti/Pt/Au metallization. Ti/Al/Mo/Au metallization was developed as a robust ohmic contact metallization for n- $Al_xGa_{1-x}N$ with x up to 0.6.

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Sincerely,

1. Foreword

GaN and related materials are novel materials that have essentially become "universal" semiconductors due to their usefulness in a broad range of device applications. With the new results on InN bandgap pointing to a value of 0.8 eV, it means that engineered AlInGaN materials may be capable of optical emission/detection from deep UV to infrared wavelengths. From high power HFETs to laser diodes and light emitting diodes, GaN materials will be ubiquitous in the future! Therefore, process development for these classes of devices is very important. The research reported here has dealt primarily with process development and has built on the activities that have been carried out in the Principal Investigator's Laboratory since 1988.

The PI wishes to acknowledge the support of DARPA in this research and the support of the Program managers and Monitors during the execution of the work herein reported. Thanks are due Dr. Robert Leheny, Dr. Edgar Martinez, Dr. Nadia El Masry, and Dr. William Clark.

2. Table of Contents

3. Statement of the Problem Studied

Many obstacles have traditionally prevented the realization of high performance devices in $Al_xGa_{1-x}N$ materials. These impediments include low material quality, lack of low-damage etching methods, lack of high temperature Schottky and ohmic metallizations, p-type ohmic metallizations with low contact resistance, and the need for effective passivation materials. Over the last decade, concentrated efforts have enabled significant improvements in the quality of GaN epitaxial materials and techniques such as lateral epitaxial growth have made possible reliable optical devices. Commensurate efforts are required to develop viable processing technologies for devices in GaN materials. The physical and chemical properties of GaN materials are sufficiently different from those of other conventional III-V semiconductors such that the processing techniques needed for both sets of materials are equally different. Indeed, it is difficult to adapt the methodologies developed for III-V processing in a wholesale fashion for GaN device realization. It is imperative to develop optimum processing technologies for GaN materials. Therefore, our work under the DARPA grant involved the development of processing techniques for GaN and related materials.

Specifically, we have studied:

i) low-damage dry etching of $Al_xGa_{1-x}N$ using inductively-coupled-plasma reactive ion etching (ICP-RIE),
ii) wet etching of n-GaN using photoelectrochemical (PEC) etching,
iii) high temperature, high Schottky barrier-height metallizations,
iv) ohmic contact metallization with low resistance on n-type and p-type $Al_xGa_{1-x}N$.

3.A Low-damage Dry Etching of $Al_xGa_{1-x}N$

Inductively-coupled-plasma reactive ion etching (ICP-RIE) is a high density plasma technique carried out in a reactor such as illustrated in Fig. 1. The plasma is inductively generated via coils that are excited at 2 MHz. This method of coupling results in a higher efficiency of plasma generation and it also means that plasma can be generated and sustained in a higher vacuum environment than possible for conventional RIE tools. The independent biasing of the sample with a 13.56 MHz generator provides for the control of the energy at which ions bombard the sample. The directionality of low energy ions is preserved due to higher vacuum environment. This means that anisotropy can be achieved for etch profiles at lower ion energies.

In our work, we have obtained high etch rates as shown in Fig. 2 (a) which displays etch rates as a function of bias voltage for $Al_xGa_{1-x}N$ with various x values. The high etch-rates produced by the ICP-RIE method are due to the higher plasma density available. The etch yields in the high-density plasma tools are the same as those in conventional RIE system, but the much larger ion fluxes in the former lead to higher etch rates. The etch rates are cast in Fig 2 (b) as a function of x in $Al_xGa_{1-x}N$. It is seen that etch rates decrease as a function of x. The decrease is due to the increasing bond energy as x

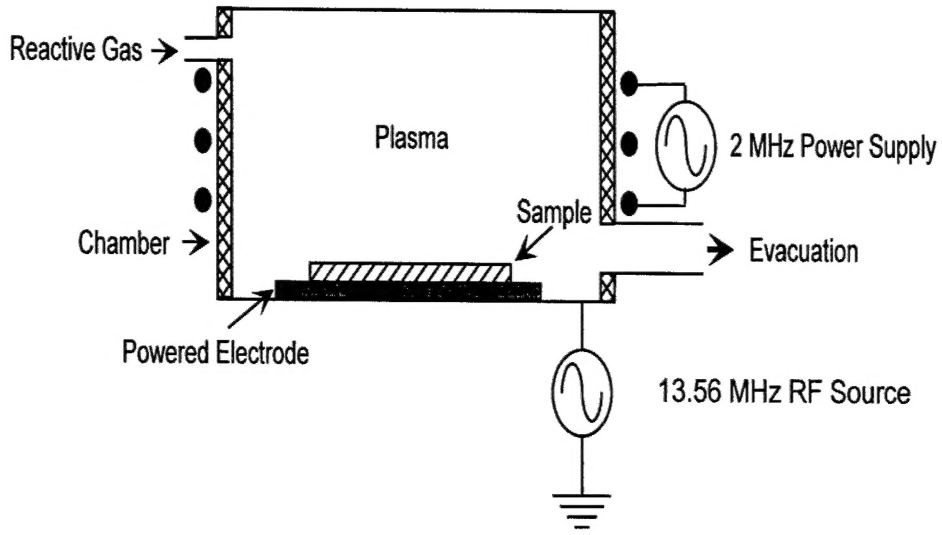

Fig. 1 Schematic diagram of an inductively-coupled-plasma reactive ion etching system.

increases. More ion energy is needed to break the bonds as x increases and this dependence on x differs from the etching of such compounds as $Al_xGa_{1-x}As$ where equi-etch rates can be obtained for various compositions [1]. Figure 2 shows etch rate of n-GaN as a function of ICP coil power for different bias voltages. As seen, the etch rate was found to be dependent on both the ICP coil power and the bias voltage. Both these parameters signify that the etch rate depend in a complex fashion on density of the ionized gaseous species and the ion energy in the chamber [2]. Using a silicon dioxide/chrome composite mask, etch profiles were studied. By balancing physical and chemical etching mechanisms, a resulting optimum profile obtained for an etched GaN/InGaN/AlGaN heterostructure is shown in Fig. 3 [1]. The etched sidewalls were engineered to be smooth and the planar etched surface was also smooth.

Damage is a critical issue on etched surfaces. To assure that the composition of etched surfaces is stochiometric, Auger electron microanalysis was performed and it was found that after etching a slight native oxide clean in HCl/H_2O was necessary. On such surfaces, we fabricated Schottky diodes to probe any processing induced-damage electrically. It was found that the key parameter responsible for damage was the sample bias voltage. Figure 4 shows the dependence of various parameters – Schottky barrier height, reverse voltage, forward voltage, and ideality factor on bias voltage. It is seen that these parameters decrease as the bias voltage increases [2]. To restore the parameters to the pre-etch characteristics, it was necessary to anneal at ~ 700 °C for 1 minute.

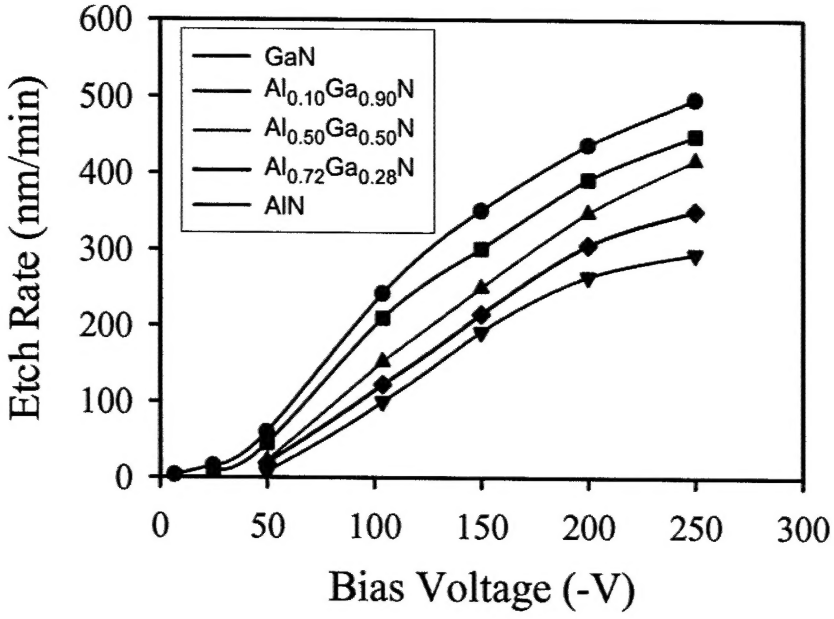

Fig. 2a Summary of etch rate of $Al_xGa_{1-x}N$ as a function of the bias voltage.

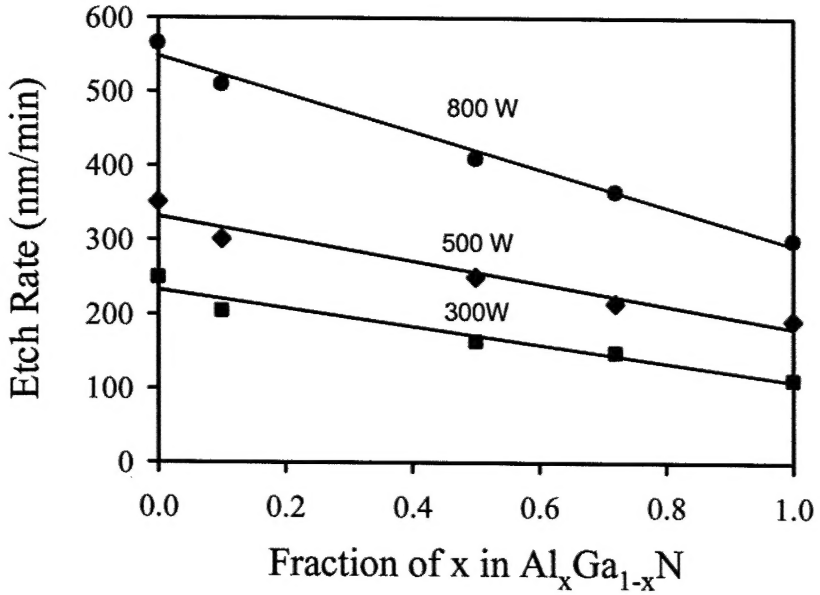

Fig. 2a Summary of etch rate of $Al_xGa_{1-x}N$ as a function of the Al mole fraction with varying ICP coil power.

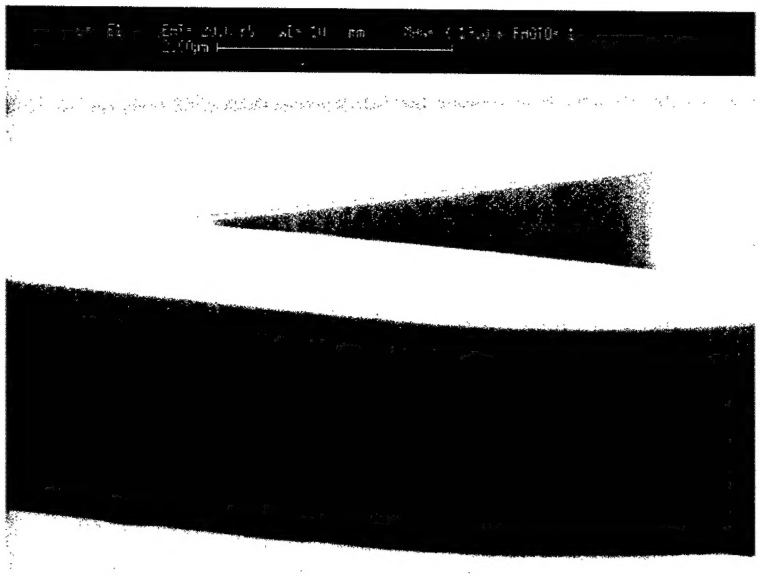

Fig. 3 Etching profile of GaN/InGaN/AlGaN heterostructure using ICP-RIE.

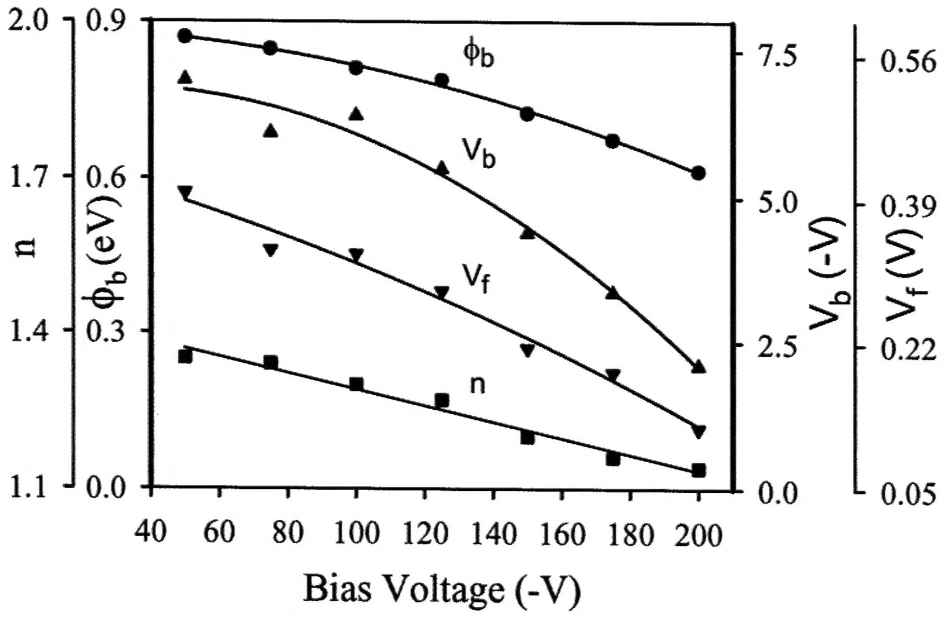

Fig. 4 Variation of Schottky barrier height (ϕ_b), ideality factor (n), reverse breakdown voltage (V_b) and forward turn-on voltage (V_f) of Schottky diode on GaN as a function of the ICP-RIE self-bias voltage.

3.B Wet Etching of n-GaN using photoelectrochemical etching

We have investigated the wet etching of GaN using the photoelectrochemical (PEC) technique. At this point, etching has been observed to occur in n-GaN but not in p-GaN. We have not conducted consistent experiments on the etching of n-AlGaN due to unavailability of high quality materials. The etching of n-GaN was conducted in a simple electrochemical cell with no bias applied as shown in Fig. 5. The GaN samples were illuminated during the etching by a 350 W Hg lamp. The electrolyte consisted of dilute aqueous solutions of KOH with various concentration (pH) values. The solutions were magnetically stirred. Etching was obtained only when optical radiation was present and it was monitored during etching by recording the current flow through the circuit. Etch rates were measured using a Tencor Alphastep system and etch morphologies were observed in a scanning electron microscope. Figure 6 shows etch rate values as a function of pH values at different incident optical intensities. The limitation in etching at low pH is due to the low concentrations of etching reactants while the rate limiting mechanism at high pH values is the inadequate removal of the gallium oxides formed as the intermediate step in the etching process.

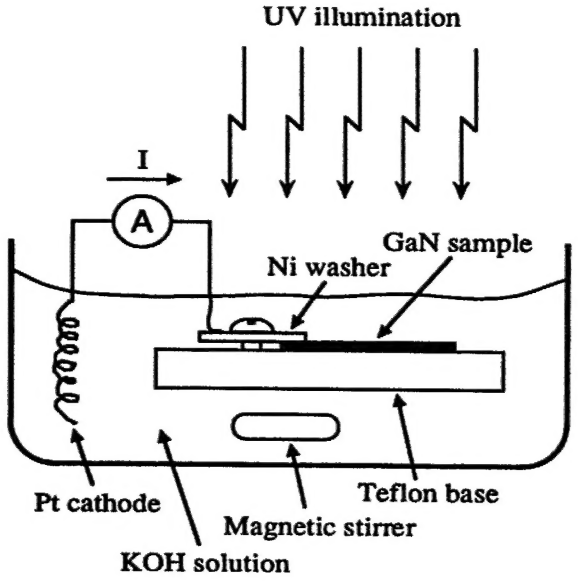

Fig. 5 Schematic diagram of an electrochemical cell used for photoelectrochemical etching of n-GaN in KOH.

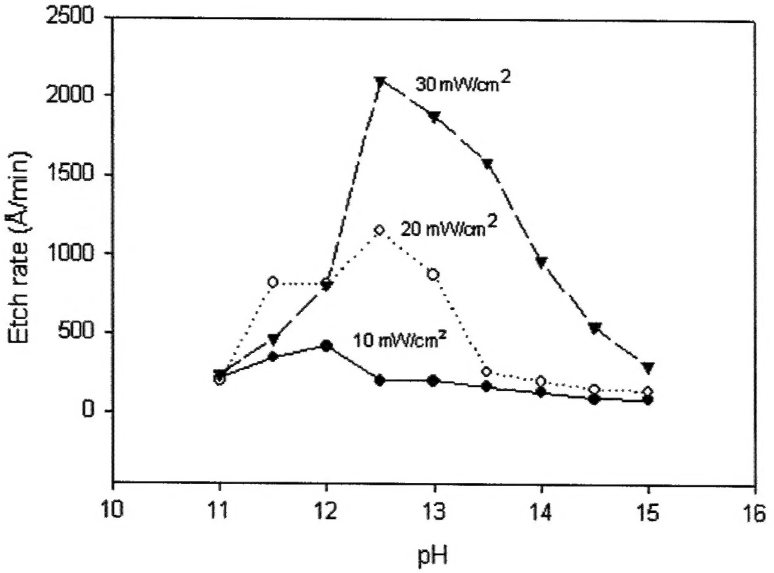

Fig. 6 Summary of etch rates of PEC etching of GaN as a function of pH of KOH electrolyte solution and incident UV light power intensity.

Surface morphologies observed were dependent on optical intensity and pH value. Three significant morphologies observed are illustrated in Figure 7 which ranged from a) smooth etched surface obtained at pH < 12, b) dislocation decoration at pH of ~ 12.5 to 13.0, and c) large hexagonal pits at high pH values. The mechanisms responsible for all these myriads of surface morphologies are still not completely understood. However, the dislocation decoration of Fig. 7 (b) is due to the fact that the "nanowhiskers" observed have at their cores mixed or edge threading dislocations [3]. This is demonstrated in the transmission electron micrograph shown in Fig. 8. The diameter of individual dislocation "whiskers" is less than 50 nm, a plan view of a dislocation in a scanning electron microscope will be a spot or dot. Therefore an aerial image over a large area results in the type of "star map" shown Fig. 9. The counting of dots in a fixed area of the map yields the dislocation density of the material. Figure 9 shows the dislocation map of a high defect density MOCVD-grown n-GaN on SiC. The sample was etched in 0.004 M KOH under 30 mW/cm^2 light intensity for 15 min. The dislocation density is estimated from the figure to be 3.2×10^9 cm^{-2}. This estimation has been verified using TEM. It is seen that PEC method can be utilized for a rapid evaluation of dislocation densities in n-GaN materials. This method is less tedious than the conventional TEM method of assessing dislocation densities.

Although, we have demonstrated the fabrication of a device using wet etching [4], it has in general been difficult to utilize PEC etching to consistently fabricate devices. The utility of PEC etching at this point may rest on its efficacy for material characterization.

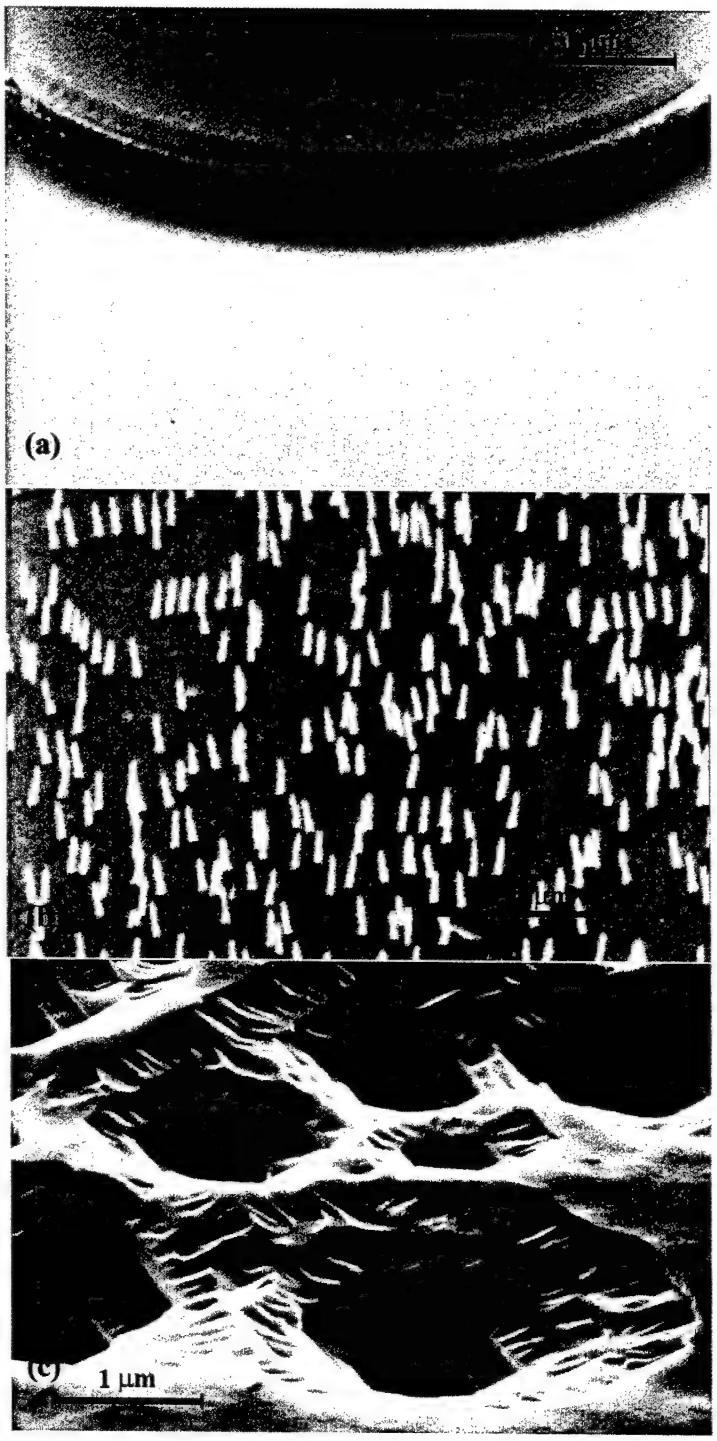

Fig. 7 Surface morphology of PEC etched GaN under obtained by varying etch conditions such as pH of KOH solution and intensity of UV illumination. The surface morphology varied from a smooth surface shown in Fig. 7(a) and dislocation decorated surface shown in Fig. 7(b) to large hexagonal etch pits shown in Fig. 7(c)

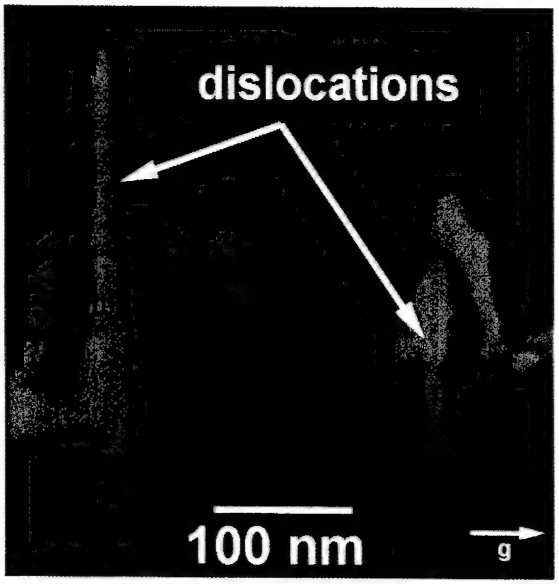

Fig. 8 Cross-sectional TEM image of a nanowhisker showed the presence of edge threading and mixed dislocations in the core of the nanowhisker.

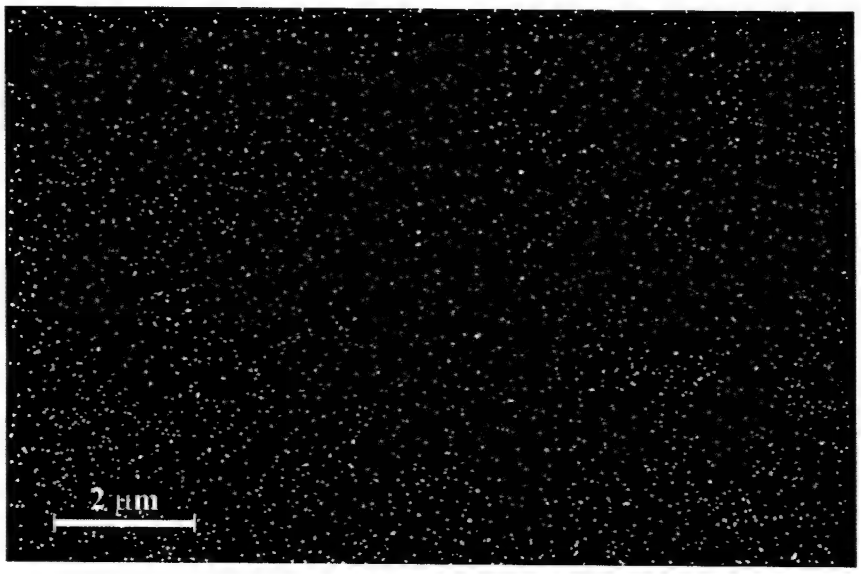

Fig. 9 Dislocation map of a high defect density MOCVD-grown n-GaN on SiC. The sample was etched in 0.004 M KOH under 30 mW/cm^2 light intensity for 15 min. The dislocation density is estimated from the figure to be 3.2×10^9 cm^{-2}.

3.C Schottky Barrier Heights of various metals on $Al_xGa_{1-x}N$

The formation of Schottky contacts in important for photodetectors, and in particular, the values of Schottky barrier heights for various metals on $Al_xGa_{1-x}N$ are not really well known. We have conducted experiments on the measurements of barrier heights of some metals on $Al_xGa_{1-x}N$ for x between 0 and 0.20. The $Al_xGa_{1-x}N$ layers used for this study consisted of 3 μm-thick undoped $Al_xGa_{1-x}N$ followed by 1 μm of Si-doped $Al_xGa_{1-x}N$. Bulk carrier concentrations of the doped layers were determined by current-capacitance (C-V) measurements to be about 2.5×10^{17} cm^{-3}. The GaN layer used had a similar structure with a nominal bulk carrier concentration of 1.4×10^{17} cm^{-3}. The measured device structure consisted of an array of 250 μm diameter Schottky dots separated 25 μm radially from the Ti/Al-based ohmic contact. Prior to transferring the samples into the metal evaporation chamber, $Al_xGa_{1-x}N$ surfaces were cleaned with an O_2 plasma asher, followed by dips in dilute HF:DI solutions. Thermal or electron beam evaporation was used to deposit the various metals to thicknesses above 80 nm. After fabrication, Schottky diode characteristics were measured using current-voltage (I-V), C-V, and modified Norde (I-V-T) techniques.

A summary of the results obtained is shown in Table 1. Results for Au, Co, Cu, Ni, Pd, Pt, and Re are shown. The I-V-T labeled as the modified Norde plot yielded barrier heights that are more consistent with the I-V method. Barrier heights obtained by C-V measurements were too high for higher x because of higher series resistances. In general, for each metal, barrier height increases with increasing x, which shows that the Fermi level is not pinned as obtains in GaAs. The C-V measurements were conducted at 1 MHz. Preliminary work has been done on multi-frequency C-V measurements. The results obtained at 40 KHz for Re, Ni, and Pt are tabulated in Table 2. It is seen that the barrier heights obtained at 40 KHz are more in agreement with the other methods. More work needs to be done on these metals when more uniform materials are available.
Temperature stability of some metals has been investigated. The metal that we have obtained extensive results on is Re [5] and these are shown in Fig. 10. It is observed that Re on GaN is thermal stable up to 800 °C with the barrier height essentially remaining the same or increasing slightly. For $Al_{0.10}Ga_{0.90}N$, degradation starts occurring at 600 °C, while for $Al_{0.26}Ga_{0.74}N$, the barrier height starts decreasing at 500 °C. It means that Re can be utilized on materials with x less than 0.26 where thermal stability up to 500 °C is desired. Further work on the formation of contacts on materials of higher x values is required for completeness.

3.D p-type ohmic contacts on $Al_xGa_{1-x}N$

There are several challenges in obtaining excellent ohmic contacts on p-$Al_xGa_{1-x}N$ materials. The low solubility of Mg in $Al_xGa_{1-x}N$ and the large acceptor binding energy militates against the achievement of high doping density. The conventional metallization for p-GaN metallization is Ni/Au, however it is very difficult to obtain contact resistivity below 1×10^{-3} ohm-cm^2. The push is to obtain superior contact resistivities and some techniques that we have explored to improve the resistivities include: surface cleaning,

Schottky metal	Al%	I-V		C-V		Modified Norde Plot		
		n	$q\phi_{BF}$ (eV)	$N_d \times 10^{17}$ (cm^{-3})	$q\phi_{bcv}$ (eV)	R_s (Ω)	A^{**} ($Acm^{-2}K^{-2}$)	$q\phi_b$ (eV)
Au	0%	1.18	1.127	2.1	1.171	56.5	55.6	1.122
	10%	1.22	1.272	2.0	1.248	279	9.26	1.240
	15%	1.48	1.368	1.6	1.891	501	21.0	1.363
	20%	1.19	1.511	1.3	3.337	2310	16.0	1.501
Co	0%	1.32	1.128	1.9	1.144	57.5	3.8	1.070
	10%	1.26	1.282	1.8	1.179	316	1.6	1.194
	15%	1.21	1.289	1.6	1.550	576	19.7	1.280
	20%	1.14	1.360	1.4	2.595	1804	0.06	1.180
Cu	0%	1.21	0.972	2.1	0.998	49.9	2.2	0.992
	10%	1.25	1.104	2.0	1.071	256	12.2	1.082
	15%	1.29	1.319	1.7	1.511	596	143	1.438
	20%	1.33	1.399	1.1	4.115	3751	0.1	1.183
Ni	0%	1.21	1.193	1.8	1.292	186	9.4	1.155
	10%	1.25	1.380	2.7	1.350	554	1.9	1.290
	15%	1.39	1.387	1.4	1.564	961	9.8	1.376
	20%	1.15	1.528	1.8	1.931	1716	0.007	1.280
Pd	0%	1.22	1.324	2.1	1.437	n/a	n/a	n/a
	10%	1.46	1.491	2.6	1.580	n/a	n/a	n/a
	15%	1.42	1.537	1.7	2.109	n/a	n/a	n/a
	20%	1.34	1.955	1.4	2.976	n/a	n/a	n/a
Pt	0%	1.18	1.110	2.1	1.207	61	26.2	1.233
	10%	1.35	1.326	2.2	1.235	239	52.1	1.360
	15%	1.14	1.378	1.7	1.734	551	7.4	1.340
	20%	1.23	1.475	1.1	3.557	2464	2.5	1.400
Re	0%	1.31	1.127	2.1	1.079	76	22.7	1.130
	10%	1.27	1.240	2.3	1.183	497	1.3	1.140
	20%	1.23	1.447	1.4	2.461	1547	2.1	1.365

Table 1 Summary of Schottky diode characteristics of devices fabricated on $Al_xGa_{1-x}N$ with different Schottky metal contacts such as Au, Co, Cu, Ni, Pd, Pt and Re. The diode characteristics were obtained from I-V, C-V and I-V-T measurements.

Schottky metal	Al%	I-V		C-V 1Mhz (40kHz)		Modified Norde Plot		
		n	$q\phi_{BF}$ (eV)	$N_d \times 10^{17}$ (cm^{-3})	$q\phi_{bcv}$ (eV)	R_s (Ω)	A^{**} ($Acm^{-2}K^{-2}$)	$q\phi_b$ (eV)
Re	0%	1.31	1.03	2.1 (2.1)	1.08 (1.06)	76	22.7	1.130
	10%	1.27	1.24	2.3 (2.2)	1.18 (1.14)	497	1.3	1.140
	15%	1.29	1.27	1.7 (1.7)	1.50 (1.19)	1030	2.1	1.365
	20%	1.23	1.32	1.4 (1.4)	2.46 (1.20)	2547	2.1	1.365
Ni	0%	1.21	1.19	1.8 (1.9)	1.29 (1.28)	186	9.4	1.155
	10%	1.25	1.28	2.7 (2.6)	1.35 (1.30)	554	1.9	1.290
	15%	1.39	1.29	1.4 (1.5)	1.56 (1.40)	961	9.8	1.376
	20%	1.25	1.23	1.8 (1.8)	1.93 (1.26)	1716	0.007	1.280
Pt	0%	1.18	1.21	2.1 (2.1)	1.21 (1.20)	61	26.2	1.233
	10%	1.25	1.33	2.2 (2.0)	1.34 (1.30)	239	52.1	1.360
	15%	1.34	1.38	1.7 (1.7)	1.53 (1. 35)	551	7.4	1.340
	20%	1.23	1.39	1.1 (1.1)	3.56 (1.34)	2464	2.5	1.400

Table 2 Summary of Schottky diode characteristics of devices fabricated on $Al_xGa_{1-x}N$ with different Schottky metal contacts such as Re, Ni and Pt. The diode characteristics were obtained from I-V, variable frequency C-V and I-V-T measurements.

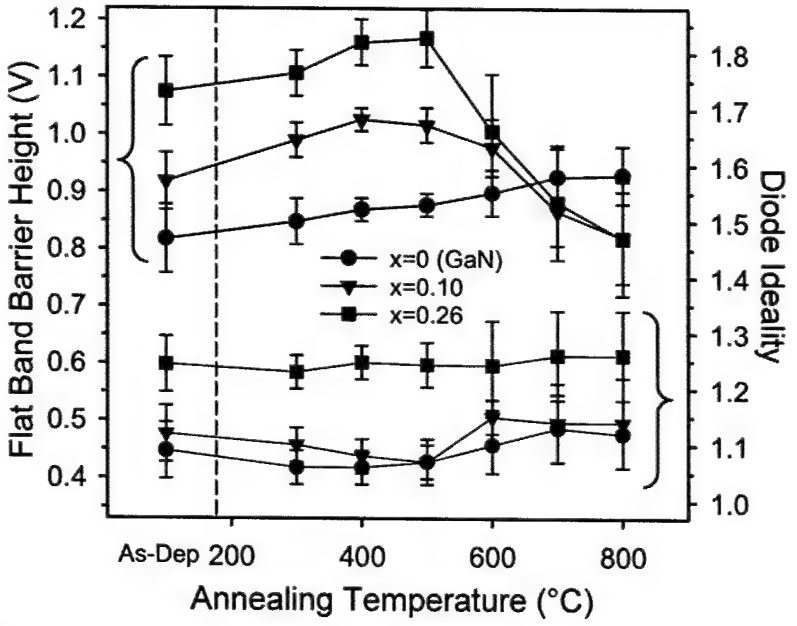

Fig. 10 Thermal stability of Re Schottky diodes obtained from flat band barrier height and diode ideality factor measurements as a function of the anneal temperature.

use of oxygen scavenging metal such as Ti and Pd, and the use of p-AlGaN/GaN superlattice layer to improve p-type sheet hole concentration.

a. Cleaning of GaN and AlGaN Surfaces

The cleaning of GaN and AlGaN surfaces are very crucial in device fabrication. Issues of residual surface contaminations and stoichiometries are important in ohmic contact formation. Therefore, we studied the surfaces of GaN and AlGaN samples cleaned in three commonly used wet chemicals. The samples were dipped in NH_4OH, HCl, and buffered oxide etch (BOE) and then rinsed in water before been blown dry. The surfaces were probed using x-ray photoelectron spectroscopy (XPS) with particular attention paid to the residual oxides on the surfaces. On the GaN, the as-received and the NH_4OH-cleaned samples exhibited surface oxides whereas the HCl- and BOE-cleaned surfaces were essentially free of oxides as shown in Figs 11 (a) and (b). For AlGaN, as-received and NH_4OH-cleaned samples exhibited residual oxides. Although HCl cleaning was more effective than NH_4OH, there was still some residual oxides on the HCl-cleaned samples. BOE was the most effective cleaning agent for the AlGaN removing any traces of oxides. Cleaning with BOE also seems to offer some passivation to GaN and AlGaN surfaces for many hours after the cleaning had been completed. The BOE cleaning described has been utilized in the preparation of p-GaN ohmic contacts.

In utilizing it, a two-step process was adopted where BOE is first used to clean the GaN wafer prior to resist spinning and lithography and another BOE clean was performed just prior to metallization. This method has proven effective in yielding better performing Ni/Au ohmic contacts on p-GaN than HCl clean [6].

b. Ti/Pt/Au ohmic contacts on p-type GaN

Titanium is known to be effective in reducing surface contaminants on semiconductors and to that effect it was adopted as the immediate contact layer for reducing any oxides on the surface of p-GaN even after cleaning. Platinum is a high work-function material well suited for ohmic contact formation to p-GaN. Gold is utilized as a cap layer to protect underlying metallization during annealing and to enhance conductivity. Ti/Pt/Au was studied as ohmic metallization on p-type GaN [7]. The GaN used was grown by MOCVD on sapphire substrates. The GaN was 0.3 μm thick and it was grown on 3 μm-thick undoped GaN. The activated dopant concentration was $\sim 2.5 \times 10^{17}$ cm^{-3} and the mobility was 9 $cm^2/V.s$. The surface of the sample was cleaned in HCl/H_2O prior to metallization with 15 nm Ti/50 nm Pt/80 nm Au. Post-deposition heat treatment was carried in a nitrogen atmosphere in an RTA system. Measurements from TLM patterns were made and the I-V characteristics across a 3 μm gap are shown in Fig. 12 for various annealing temperatures. It is seen that the linearity of the I-V curves improved with higher annealing temperatures. The lowest contact resistivity obtained was 4.2×10^{-5} ohm-cm^2 for contacts annealed at 800 °C for 2 min. The use of Ti does demonstrate its efficacy in neutralizing the effects of contamination/oxide layer on the p-GaN surface. The major obstacle to the adoption of this process is that the thickness of Ti is very important and may need to be adapted to various layers and cleaning procedure.

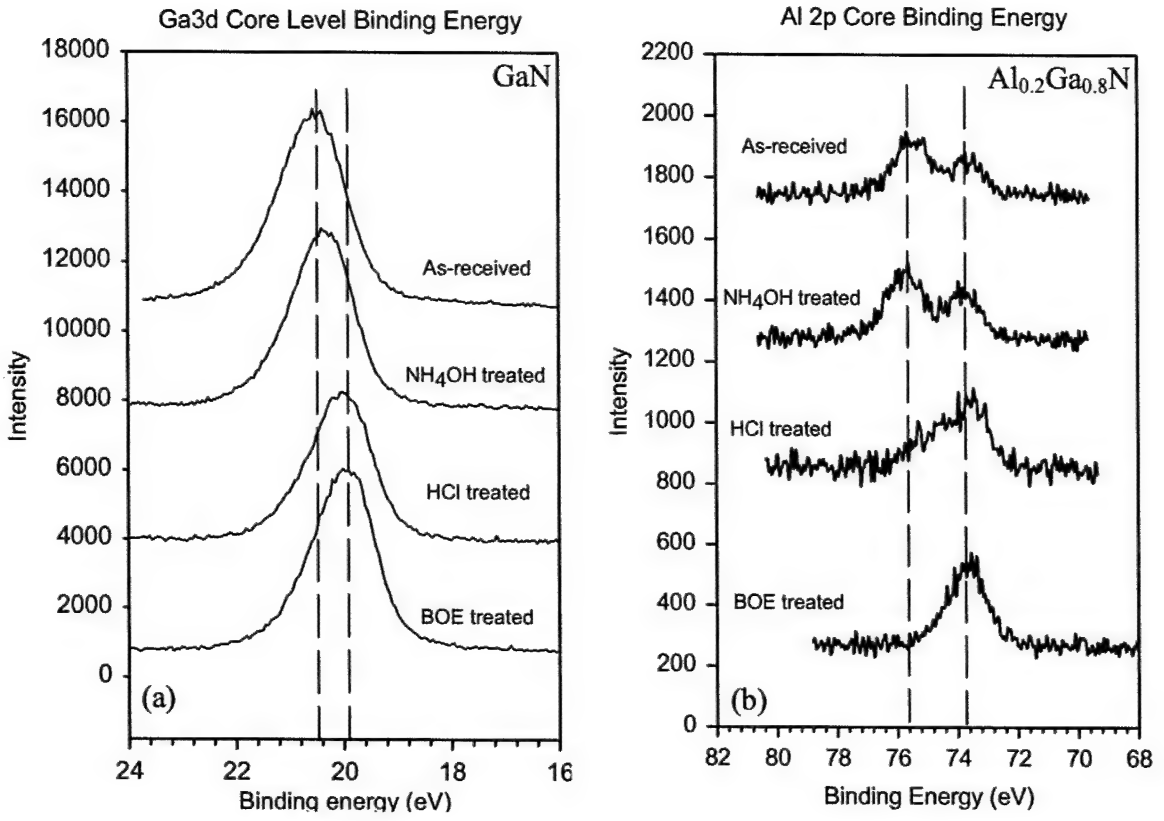

Fig. 11 X-ray photoelectron spectra of Ga 3d and Al 2p level in GaN and $Al_{0.2}Ga_{0.8}N$ for various surface treatment mechanisms to reduce the native surface oxide concentration.

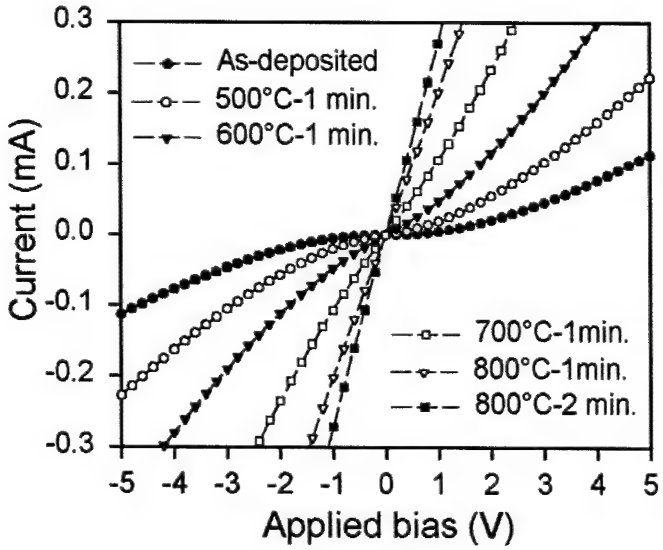

Fig. 12 I-V characteristics for Ti/Pt/Au contacts on p-GaN with a 3 μm gap spacing, as a function of the anneal temperature.

c) Ti/Pt/Au ohmic contacts on p-type $GaN/Al_xGa_{1-x}N$ superlattices

The overall hole concentration in a p-type can be increased through the generation of valence band edge oscillations in a superlattice as proposed Schubert et al. [8]. The technique improves the activation efficiency of deep acceptors. This method has enabled the realization of enhanced p-type doping efficiency in $GaN/Al_xGa_{1-x}N$ superlattices [9]. We have investigated Ti/Pt/Au ohmic contacts on $GaN/Al_xGa_{1-x}N$ superlattices. The superlattice layers used were grown by MBE on sapphire and consisted of 20 periods each of Mg-doped GaN (10 nm) and $Al_xGa_{1-x}N$ (10 nm). Samples with two different Al concentrations, x=0.1 and 0.2, were investigated. The samples exhibited a mobility of 1 $cm^2/V.s.$ as determined by room temperature hall measurements. TLM patterns were fabricated on the samples using Ti/50 nm Pt/80 nm Au metallization and the I_V characteristics were measured at room temperature. Figure 13 shows the I-V characteristics for the superlattices as compared with a reference p-type GaN ($p = 2.5 \times 10^{17}$ cm^{-3} and $\mu = 9$ $cm^2/V.s.$) also investigated at room temperature. The as-deposited contact is rectifying on the reference p-GaN. In contrast, owing to the enhanced doping efficiencies, the I-V curves for $GaN/Al_xGa_{1-x}N$ superlattices exhibit better linearity. The sample with the higher Al content ($x = 0.2$) was more ohmic in its I-V characteristics. This is consistent with a high carrier concentration expected for the superlattice with $x = 0.2$ than for the other with $x = 0.1$. The ohmic contact resistivities are 6.6×10^{-4} and 4.6×10^{-4} ohm-cm^2 for $x = 0.1$ and $x = 0.2$, respectively. Thermal treatments of the ohmic contacts beyond 300 °C resulted in degradation. The underlying cause of the degradation was not resolved. The major issue might have been due to the fact that the superlattices utilized in our study terminated in the AlGaN layer. It will be useful to study layer that are terminated with doped GaN.

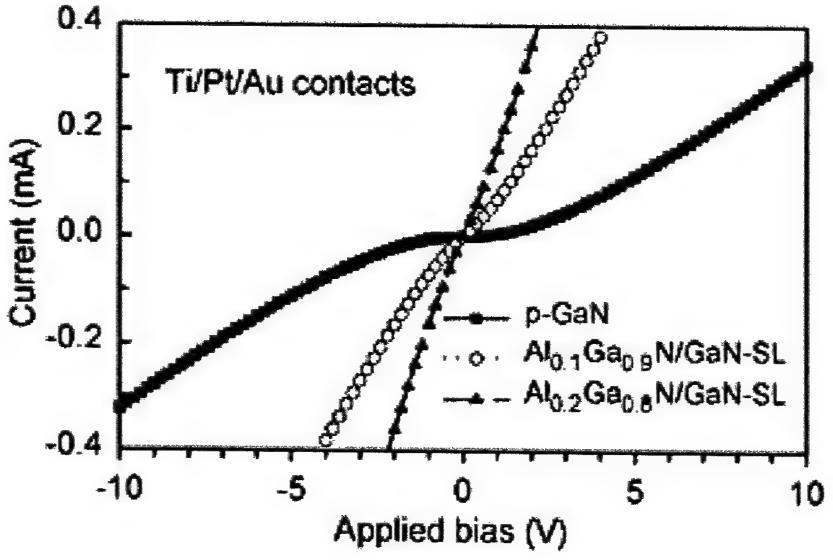

Fig. 13 I-V characteristics of as-deposited Ti/Pt/Au contacts on p-GaN and Al_xGa_{1-x}/GaN SL with $x \sim 0.10$ and 0.20.

3.E n-type ohmic contacts on $Al_xGa_{1-x}N$

Ohmic contact formation on n-type GaN has been easier than what obtains for p-type GaN. This is due to the fact that the achievable level of carrier density is much higher. However, much like the p-$Al_xGa_{1-x}N$, the incorporation and ionization of Si donors become problematic as x increases, therefore ohmic contact formation at high x values is challenging. The requirements for excellent ohmic contacts include low contact resistance, smooth surface morphology, excellent thermal stability, and good edge acuity. The commonly used n-type ohmic metallization is Ti/Al/Ti/Au where Al is the actual active component for contact formation while the Ti underlying Al is for adhesion and for reducing the surface contaminants. The Ti/Au overlayer has two functions: to passivate the Al from forming aluminum oxide during the anneal process and to improve the electrical conductivity. In addition, the Ti underneath Au should ideally serve as a diffusion barrier. However, the solubility of Au in Ti is very high such that the high reactivity of Ti and Au and also Al and Au promote lateral diffusion and very rough surface morphology for Ti/Al/Ti/Au ohmic contacts on n-GaN. Other metallizations that have been utilized to surmount these problems are Ti/Al/Ni/Au and Ti/Al/Pt/Au. The solubility of Au in Ni and Pt are still relatively high, therefore, we have developed a metallization using Mo as the diffusion barrier.

We illustrate the lateral diffusion observed for Ti/Al/Ti/Au metallization in Fig. 14 where metal has creeped into the gap between two TLM pads. X-ray analysis (EDAX) have been performed on the metallization within the gap and Au, Al, and Ti have been detected. Figure 15 shows a corresponding Ti/Al/Mo/Au metallization exhibiting excellent edge acuity. X-ray diffraction (XRD) spectra for both Ti/Al/Ti/Au and Ti/Al/Mo/Au are displayed in Fig. 16. It is seen that an array of AlAu intermetallics are formed in the Ti/Al/Ti/Au contacts in contrast to that of Ti/Al/Mo/Au where none is found. These results are due to the fact that Au has less than 1 % solubility in Mo, and therefore, Mo acts as an effective diffusion barrier [10, 11]. We have investigated ohmic contact formation as a function of Mo thickness as shown in Fig. 17. It is seen that Mo thickness as small as 25 nm is sufficient for obtaining excellent ohmic characteristics and surface smoothness. Thermal stability at 500 °C has been determined for Ti/Al/Mo/Au. The contact resistance remained essentially constant for 350 hours at 500 °C as shown in Fig. 18.

Working with an n-GaN with dopant concentration of 1×10^{18} cm^{-3} and mobility of 250 $cm^2/V.s.$, we have achieved ohmic characteristics with specific contact resistivities as low as 4×10^{-7} ohm-cm^2 for Ti/Al/Mo/Au metallization [10]. To obtain excellent ohmic contact resistivity, we have adopted a fabrication procedure that includes an ion-bombardment regimen in a RIE chamber using $SiCl_4$ plasma. A self-bias voltage of – 300 V has been found to yield the best ohmic contact results. Extensive Auger electron analyses have been carried out and have been published [10, 11].

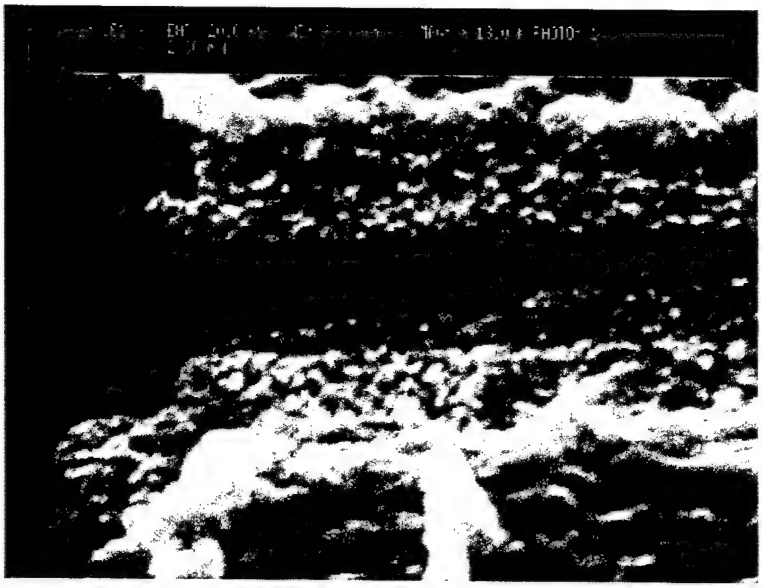

Fig. 14 Lateral diffusion of Ti/Al/Ti/Au ohmic contacts during anneal process.

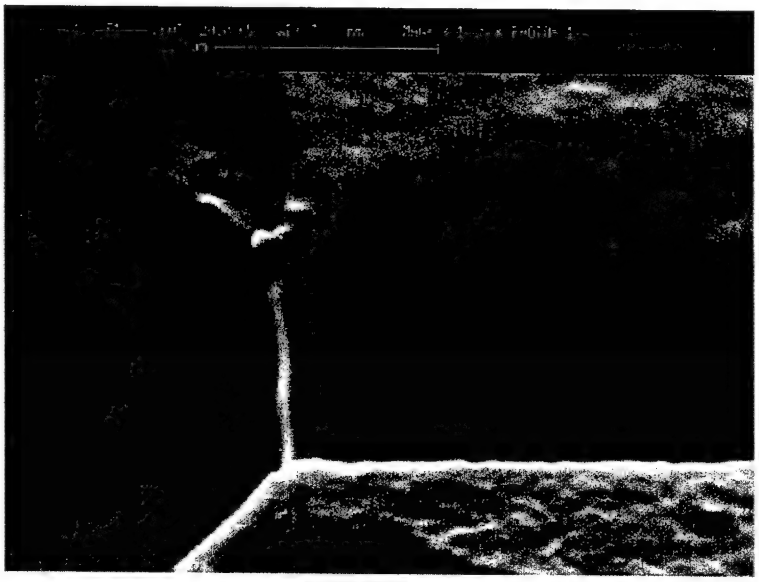

Fig. 15 Ti/Al/Mo/Au ohmic metallization exhibits sharp edge definition after annealing the contacts.

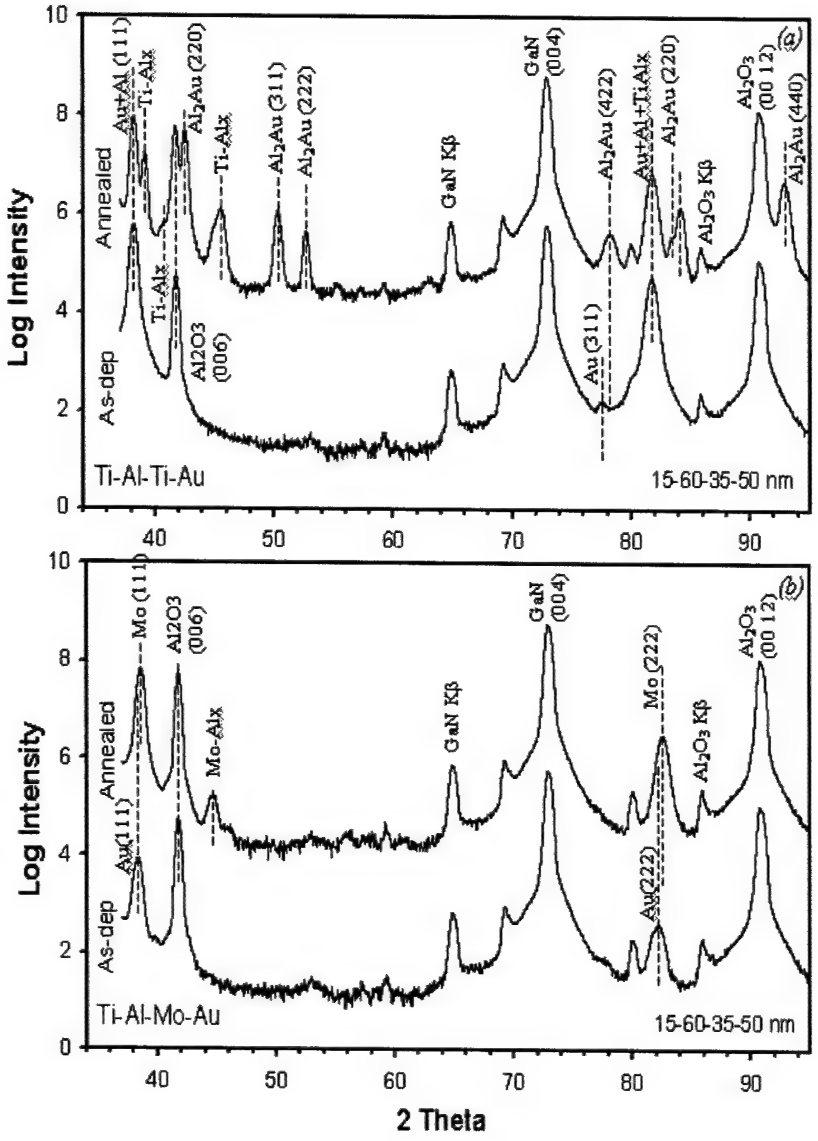

Fig. 16 XRD spectra of Ti/Al/Ti/Au and Ti/Al/Mo/Au ohmic metallization before and after anneal process. There is no evidence of Al_2Au phase in annealed Ti/Al/Mo/Au ohmic metallization when compared to Ti/Al/Ti/Au metallization scheme.

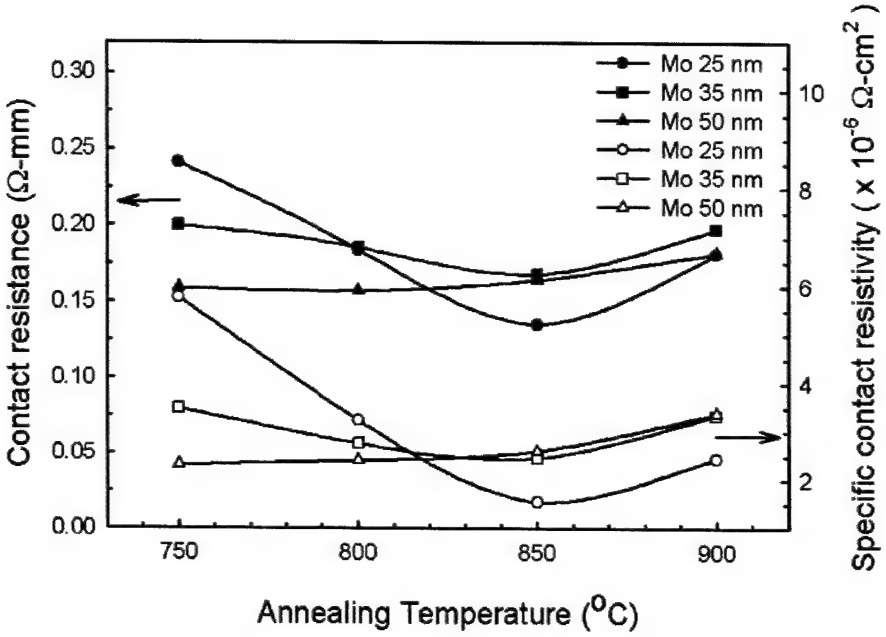

Fig. 17 Variation of contact resistance and specific contact resistivity of Ti/Al/Mo/Au ohmic contacts on n-GaN as a function of thickness of Mo.

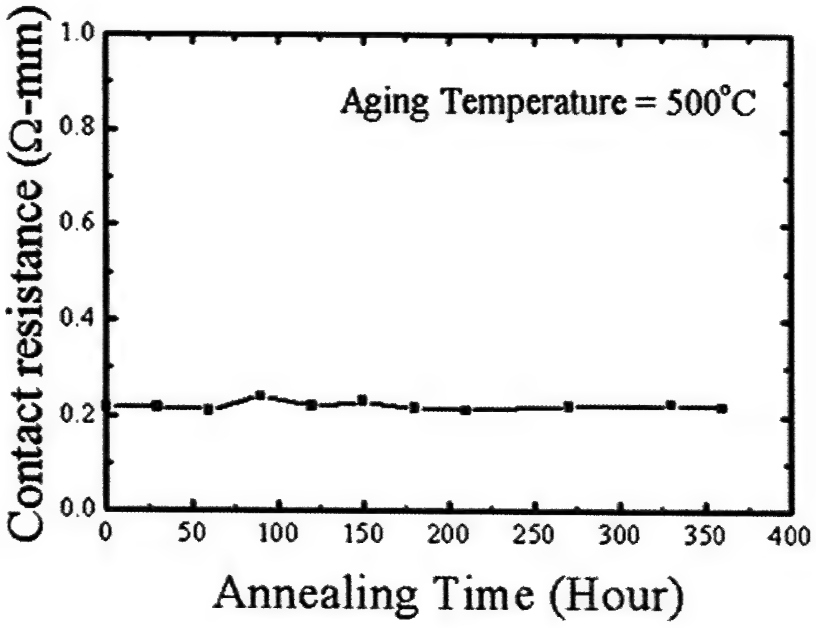

Fig. 18 Long-term thermal stability of Ti/Al/Mo/Au ohmic contacts on n-GaN.

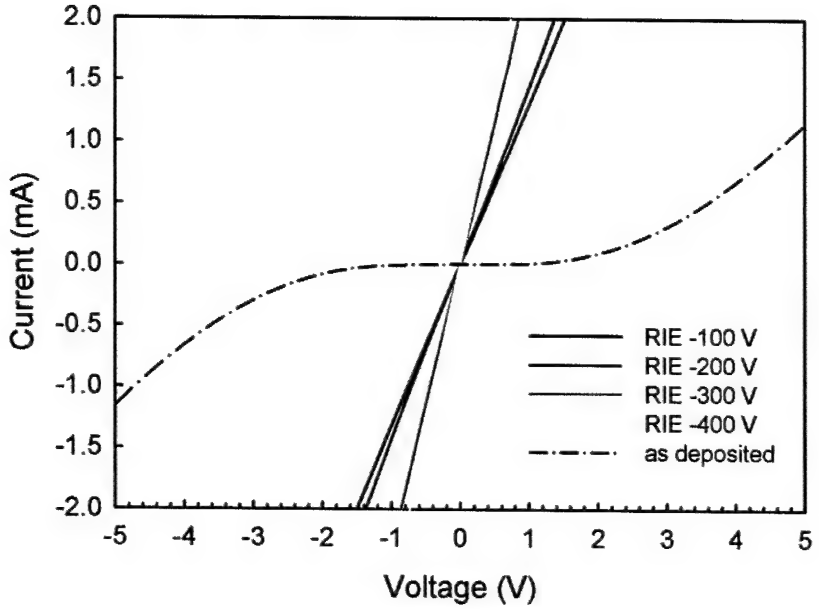

Fig. 19 I-V characteristics of as-deposited and annealed Ti/Al/Mo/Au ohmic contacts on n-$Al_{0.59}Ga_{0.41}N$ as function of the $SiCl_4$ plasma bias voltage. The contacts were annealed at 850 °C for 30 s.

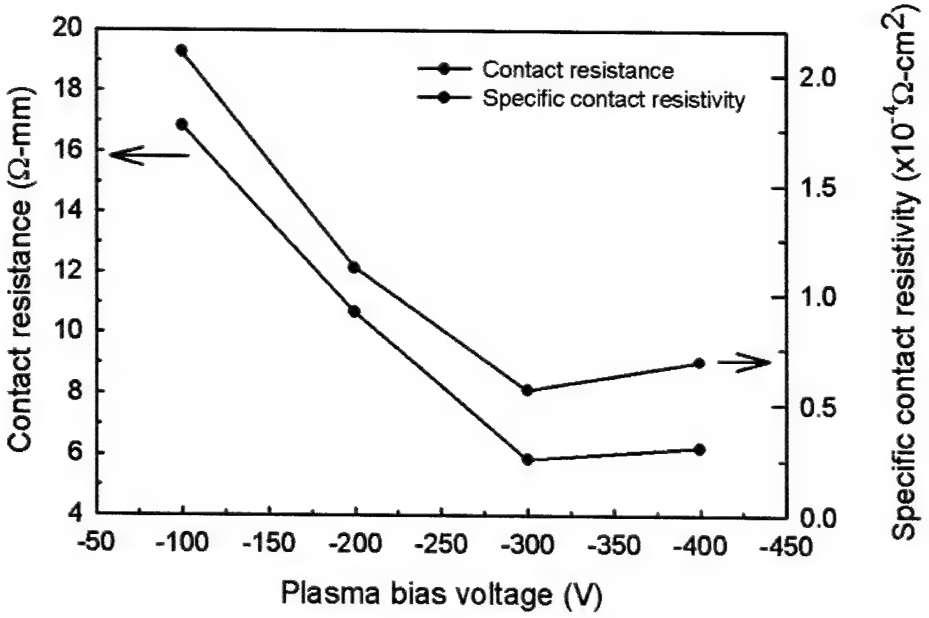

Fig. 20 Variation of contact resistance and specific contact resistivity of Ti/Al/Mo/Au ohmic contacts on n-$Al_{0.59}Ga_{0.41}N$ as function of the $SiCl_4$ plasma bias voltage. The contacts were annealed at 850 °C for 30 s.

For $Al_xGa_{1-x}N$ with higher x values, ohmic contacts are difficult to achieve. However, using Ti/Al/Mo/Au metallization, we have demonstrated excellent ohmic contact resistance for $Al_{0.59}Ga_{0.41}N$ [12]. The n-type $Al_{0.59}Ga_{0.41}N$ was grown by MOCVD on sapphire. The 0.25 μm-thick AlGaN was grown on top of a 1 μm-thick undoped GaN. The AlGaN had a carrier concentration of $\sim 3 \times 10^{17}$ cm^{-3}. Figure 19 shows the linear characteristics obtained after an anneal at 850° C for 30 s. The $Al_{0.59}Ga_{0.41}N$ surface was treated with plasma processing prior to metallization and the ohmic contact resistance as a function of the ion voltage is shown in Fig. 20. These were the first results obtained for ohmic contacts on high AlGaN materials and it remains the best to date. Further investigations on ohmic contacts on these types of materials are still needed to optimize the fabrication procedure.

4. Summary of the most important results

- Photoelectrochemical etching of n-GaN: useful for material characterization. This has been validated by the rising number of publications that have followed since our results have been disseminated.

- Anisotropic etching of $Al_xGa_{1-x}N$ materials and heterostructures: Extensive characterization of inductively-coupled-plasma reactive ion etching (ICP-RIE) of $Al_xGa_{1-x}N$. Achieved high etch rates and profile control but could not achieve any measure of selectivity due to high bond energies of these materials.

- Low-resistance ohmic contacts for p-GaN: demonstrated that surface issues are critical to ohmic contact formation. Achieved ohmic contacts with low contact resistance on p-GaN. The contact resistance, r_C=4.2 × 10-5 ohm-cm2 achieved for Ti/Pt/Au on p-GaN is the lowest achieved for processes compatible for device fabrication.

- Low-resistance ohmic contacts to p-AlGaN: Achieved ohmic contacts on p-AlxGa1-xN/GaN superlattices. Contact resistivities of $\sim 4 \times 10^{-4}$ ohm-cm^2 were obtained for as-deposited Ti/Pt/Au on $Al_{0.20}Ga_{0.80}N$/GaN.

- Schottky barrier contacts on n-AlGaN: Extensive characterization of barrier heights on n- $Al_xGa_{1-x}N$ materials. Barrier heights of various metals (Au, Pd, Pt, Co, Ni, Re, and Cu) were measured. With higher x values, variable frequency C-V technique along with I-V-T methods need to be adopted for accurate measurements. Thermal stability of refractory Re metal was determined with the metal maintaining stability up to 800 °C on n-GaN.

- Low-resistance ohmic contacts on n-GaN with high thermal stability and good edge acuity: Ti/Al/Mo/Au was adopted for ohmic metallization on n-GaN in preference to Ti/Al/Ti/Au due to the low solubility of Au in Mo. Mo acted as an effective barrier layer and prevented lateral diffusion. Plasma treatment of n-GaN surfaces was shown to be critical to good ohmic contact formation.

- Low-resistance ohmic contacts on $Al_{0.59}Ga_{0.41}N$: Excellent ohmic contact formation was achieved using Ti/Al/Mo/Au on n-AlGaN with high Al content. This was the first demonstration of such a contact.

5. Publications

Peer-Reviewed Journal Papers

1. F.A. Khan, L. Zhou, A. T. Ping, and I. Adesida, "ICP-RIE Etching of $Al_xGa_{1-x}N$ for application in Laser Facet Formation," *J. Vac. Sci. Technol.* **B17**, 2750-2754 (1999).
2. C. Youtsey, L. T. Romano, and R. J. Molnar and I. Adesida, "Rapid evaluation of dislocation densities in n-type GaN films using photoenhanced wet etching," *Appl. Phys. Lett.***74**, 3537-3539, 1999.
3. A.T. Ping, D. Selvanathan, C. Youtsey, E. Piner, J. Redwing, and I. Adesida, "Gate Recessing of GaN MESFETs using photoelectrochemical etching," *Electron. Lett.* **35**, 2140-2141 (1999).
4. L. Zhou, W. Lanford, A.T. Ping, J.W. Yang, M.A. Khan, and I. Adesida, "Low resistance Ti/Pt/Au ohmic contacts to p-type GaN," *Appl. Phys. Lett.* **76**, 3451-3453 (2000).
5. L. Zhou, A. T. Ping, F. Khan, A. Osinsky, and I. Adesida, "Ti/Pt/Au ohmic contacts on p-type $GaN/Al_xGa_{1-x}N$ superlattices," *Electron. Lett.* **36**, 91-93 (1999)
6. F.A. Khan, L. Zhou, V. Kumar, and I. Adesida, "Plasma Induced Damage Study to n-GaN using ICP-RIE," *Journal of Vacuum Science and Technology* **B 19(6)**, 2926-2929 (2001).
7. L. Zhou, F. A. Khan, G. Cueva, V. Kumar, I. Adesida, M. R. Sardella, and F. A. Auret, "Thermal stability of rhenium Schottky Contacts on n-type $Al_xGa_{1-x}N$," *Applied Physics. Letters* **81**, 1624-1626 (2002).
8. V. Kumar, L. Zhou, D. Selvanathan and I. Adesida," Thermally stable low resistance Ti/Al/Mo/Au multilayer ohmic contacts to n-GaN" *Journal of Applied Physics* **92**, 1712-1714 (2002).
9. D. Selvanathan, L. Zhou, V. Kumar, J.P. Long, M.A.L. Johnson, J.F. Schetzina, and I. Adesida, "Ohmic contacts on n-type $Al_{0.59}Ga_{0.41}N$ for solar blind detectors," *Electronics Lett*ers **38 (14),** 755-756 (2002).
10. D.I. Florescu, F.H. Pollak, W.B. Lanford, F. Khan, I. Adesida, and R.J. Molnar, "Ion beam processing effects on the thermal conductivity of n-GaN/sapphire (0001)," *Journal of Applied Physics* **91**, 1277-1280 (2002).
11. Selvanathan D, Zhou L, Kumar V, Adesida I, "Low Resistance Ti/Al/Mo/Au Ohmic Contacts for AlGaN/GaN Heterostructure Field Effect Transistors", *Physica Status Solidi* **A194**, 583-586 (2002).

Papers presented at Conferences (Peer-reviewed Abstracts)

1. L. Zhou, A. T. Ping, J. Redwing, and I. Adesida, "Characterization of Rhenium Schottky on n-type $Al_xGa_{1-x}N$ at High Temperatures," *41st Electronic Materials Conference* (University of California, Santa Barbara, CA, June 1999). *J. Electron. Mater.* **28**, 67 (1999).
2. I. Adesida, C. Youtsey, D. Selvanathan, T. Pierson, A. Daga, M. Hossain, L. Romano, "Photoelectrochemical Etching of GaN for Materials Characterization and Device Fabrication," *41st Electronic Materials Conference* (University of California, Santa Barbara, CA, June 1999). *J. Electron. Mater.* **28**, 71 (1999).
3. F. A. Khan and I. Adesida, "ICP-RIE Etching of $Al_xGa_{1-x}N$ for application in Laser Facet Formation," *43rd Intl. Conf. on Electron, Ion, and Photon Beam Technology and Nanofabrication* (Marco Island, FL., June 1999).
4. I. Adesida, L. Zhou, A. Osinsky, "Ti-Based Ohmic Contacts to p-Type GaN/A1GaN Superlattices," *Proceedings of International Workshop on Nitride Semiconductors -IWN2000-* (Nagoya, Japan, September 2000) pp. 790-792. **(INVITED)**
5. I. Adesida, "Processing Issues in GaN-Based Materials and Devices" *International Workshop on the Physics of Light-Matter Coupling in Nitrides* (Saint-Nectaire, France, October 2000) **(INVITED)**
6. F.A. Khan, L. Zhou, V. Kumar, and I. Adesida, "Plasma-Induced Damage Study for GaN Using Inductively-Coupled-Plasma Reactor," *45th Intl. Conference on Electron, Ion, and Photon Beam Technology and Nanofabrication* (Washington, DC, May 2001).
7. F. A. Khan, L. Zhou, V. Kumar, and I. Adesida, "Inductively-coupled-plasma induced damage study for $Al_xGa_{1-x}N$," *Electronic Materials Conference* (Notre Dame, IN, June 2001), *Late News Paper.*
8. F. A. Khan, L. Zhou, V. Kumar, and I. Adesida, "Low Damage Etching of Silicon Carbide Using Cl_2 Based Plasmas," *Electronic Materials Conference* (Notre Dame, IN, June 2001), *J. Electron. Mater.* **30,** 61 (2001).
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10. D. Selvanathan, L. Zhou, V. Kumar and I. Adesida, "Low resistance Ti/Al/Mo/Au ohmic contacts for AlGaN/GaN HFETs," *International Workshop on Nitride Semiconductors* - IWN 2002 (Aachen, Germany, July 2002).
11. D. Selvanathan, V. Kumar and I. Adesida, "Thermal Stability of Ti/Al/Mo/Au Ohmic Contacts on n-GaN", *44th Electronic Materials Conference* (Santa Barbara,CA, June 2002); Journal of Electronic Materials **31**, 59-60, (2002).
12. D. Selvanathan, V. Kumar and I. Adesida, "Surface treatment of n-GaN for ohmic contact formation," *accepted for presentation at* Electronic Materials Conference (Salt Lake City, Utah, June 2003).

Topical Workshops and Meetings

1. I. Adesida "Processing Technologies for $Al_xGa_{1-x}N$ Optoelectronic Devices" *DARPA III-Nitride UV Emitters Study Group Emitters* (Washington, DC, April 2001)
2. I. Adesida, "Photoassisted Wet Etching on GaN" *Workshop on Challenges in Porous and Amorphous Wide Gap Semiconductors* (Corner Brook, Newfoundland, Canada, June 2001).
3. I. Adesida, " Processing Technologies for $Al_xGa_{1-x}N$ Detectors," *DARPA Solar Blind Detectors* (Washington, DC, September 2002).

Papers submitted but not published

1. D. Selvanathan, L. Zhou, V. Kumar, I. Adesida and N. Finnegan, "Long-term thermal stability of Ti/Al/Mo/Au ohmic contacts on n-GaN," *accepted for publication in Journal of Electronic Materials, May 2003.*

6. Scientific Personnel

Post-Doctoral Associates

Dr. Vipan Kumar

Graduate Students

1. Farid Khan, "High Rate Etching of Wide Bandgap Semiconductor Materials for Fabricating Novel Devices" M.S. Thesis, 1999. (Due to receive Ph.D. in 2003)
2. Noah Kim, "A Study of Schottky Contacts to Aluminum Gallium Nitride" M.S. Thesis, 2001. (now at Lucent Technologies).
3. Deepak Selvanathan (Due to receive Ph.D. in 2003)
4. Christopher Youtsey, "Photoelectrochemical Wet Etching of Gallium Nitride" Ph.D. Thesis, 1999 (now at Triquint, Inc.)
5. Ling Zhou, "Development and Characterization of Ohmic and Schottky Contacts for GaN and AlGaN Devices," Ph.D. Thesis, 2002 (now at Lumileds)

7. Inventions

I. Adesida and L. Zhou, "Method to metallize ohmic electrodes to p-type Group III Nitrides," U.S. Patent Application No 09/586,910 (filed in June 2000)

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[1] F.A. Khan, L. Zhou, A. T. Ping, and I. Adesida, "ICP-RIE Etching of $Al_xGa_{1-x}N$ for application in Laser Facet Formation," *J. Vac. Sci. Technol.* **B17**, 2750-2754 (1999).

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[6] I. Adesida, L. Zhou, A. Osinsky, "Ti-Based Ohmic Contacts to p-Type GaN/A1GaN Superlattices," *Proceedings of International Workshop on Nitride Semiconductors -IWN2000-* (Nagoya, Japan, September 2000) pp. 790-792.

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[10] V. Kumar, L. Zhou, D. Selvanathan and I. Adesida," Thermally stable low resistance Ti/Al/Mo/Au multilayer ohmic contacts to n-GaN" *Journal of Applied Physics* **92**, 1712-1714 (2002).

[11] D. Selvanathan, L. Zhou, V. Kumar, I. Adesida and N. Finnegan, "Long-term thermal stability of Ti/Al/Mo/Au ohmic contacts on n-GaN," *accepted for publication in Journal of Electronic Materials, May 2003.*

[12] D. Selvanathan, L. Zhou, V. Kumar, J.P. Long, M.A.L. Johnson, J.F. Schetzina, and I. Adesida, "Ohmic contacts on n-type $Al_{0.59}Ga_{0.41}N$ for solar blind detectors," *Electronics Lett*ers **38 (14),** 755-756 (2002).

9. APPENDIX A

Publications attached at the end of the report.

Inductively coupled plasma reactive ion etching of $Al_xGa_{1-x}N$ for application in laser facet formation

F. A. Khan, L. Zhou, A. T. Ping, and I. Adesida[a)]
Microelectronics Laboratory and Department of Electrical and Computer Engineering, University of Illinois, Urbana, Illinois 61801

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The etching characteristics of $Al_xGa_{1-x}N$ grown by metal–organic chemical-vapor deposition were investigated in an inductively coupled plasma (ICP) reactive ion etching system using Cl_2/Ar gas mixtures. Etch rate variations with substrate bias voltage, ICP coil power, chamber pressure, Cl_2/Ar gas mixture ratios, and gas flow rates were investigated. The optimum chamber pressure for etching was found to be dependent on both the substrate bias voltage and ICP coil power. Auger electron spectroscopy analysis showed that the stoichiometries of the etched $Al_{0.22}Ga_{0.78}N$ surfaces were identical, independent of the etching conditions. Etching results were successfully applied to form highly anisotropic and smooth facets in GaN/InGaN/AlGaN heterostructure laser materials.
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I. INTRODUCTION

Highly anisotropic and smooth sidewall etch processes are important in the fabrication of optoelectronic devices such as laser facets, turning mirrors, and gratings. $Al_xGa_{1-x}N$-based heterostructures are essential materials for such devices operating at short wavelengths. However, owing to their inert chemical nature and high bond energies, they are resistant to wet chemical etchants, making device patterning mostly dependent on dry etching. A number of dry etching techniques and plasma chemistries have been reported for etching a wide range of GaN-based materials.[1–14] Etch chemistries have been largely based on Cl_2 mixtures, while techniques used include chemically assisted ion-beam etching (CAIBE),[1–3] reactive ion etching (RIE),[4–7] electron cyclotron resonance reactive ion etching (ECR-RIE),[8–10] magnetron reactive ion etching,[11] and inductively coupled plasma reactive ion etching (ICP-RIE).[12–14] To date, there has been a paucity of work on the dry etching characteristics of $Al_xGa_{1-x}N$ over the entire compositional range.[15] It is essential to characterize the differences in etch rates between various layer compositions in order to tailor etching processes for optoelectronic and power electronic devices based on $Al_xGa_{1-x}N$ heterostructures. For example, the fabrication of laser facets and mirrors require processes with high etch rates and low selectivities between different layer compositions. On the other hand, gate recessing for field-effect transistors requires etch processes with low etch rates and high selectivities between layers of different compositions.

In this article, we present our work on ICP etching of $Al_xGa_{1-x}N$ over its entire compositional range using Cl_2/Ar gas mixtures. Etch rates were investigated as functions of ICP power, sample bias voltage, chamber pressure, gas mixture composition, and gas flow rate. Successful application of the etching results to form very smooth and highly anisotropic facets will also be discussed.

a)Electroic mail: adesida@capone.ccsm.uiuc.edu

II. EXPERIMENT

The $Al_xGa_{1-x}N$ films etched in this study were epitaxially grown by metal–organic chemical-vapor deposition (MOCVD) on (0001) sapphire substrates. The thickness of the GaN epilayer was 2 μm while the thickness of the $Al_xGa_{1-x}N$ ($x=0.1-1$) epilayers ranged from 0.3 to 0.8 μm. A Si_xN_y/Cr bilayer mask structure was used for the characterization of etch rates. Si_xN_y was deposited on the $Al_xGa_{1-x}N$ layers using plasma-enhanced chemical-vapor deposition (PECVD). A metal lift-off technique was then used to pattern the samples with evaporated Cr. The pattern defined by the Cr was subsequently transferred into the Si_xN_y using SF_6 plasma. Samples were cleaned briefly in a 1:1 solution of HCl:H_2O prior to being etched and the etching was conducted in a Plasma-Therm Shuttlelock 700 ICP-RIE system. A schematic of the ICP-RIE chamber is shown in Fig. 1, which consists of an inductive source mounted on a standard RIE system. A high-density plasma discharge is generated by applying rf power to the inductive coil using a 2 MHz source. The plasma diffuses from the generation region to uniformly fill the chamber and drifts to the substrate's surface at energies determined by the substrate bias voltage. The substrate bias voltage can be independently controlled by tuning the second, 13.56 MHz, rf supply connected to the stage. A gas flow mixture of 25 sccm of Cl_2 and 5 sccm of Ar was used for all experiments unless otherwise stated. All samples were etched with the stage temperature held at 28±3 °C. After etching, dilute HF was used to remove the Si_xN_y/Cr mask. A profilometer was used to measure the etch depths. Since this study was geared towards the fabrication of smooth facets, emphasis was laid on investigating processes that yielded high etch rates for $Al_xGa_{1-x}N$.

III. RESULTS AND DISCUSSION

A. Etch rate study

$Al_xGa_{1-x}N$ etch rates as a function of bias voltage are shown in Fig. 2(a). The ICP power and the chamber pressure

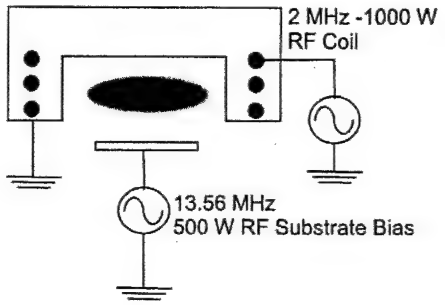

FIG. 1. ICP-RIE etching system.

were kept constant at 500 W and 5 mT, respectively. The energy of the ions incident on the surface of the substrate is dependent on the bias voltage. For all $Al_xGa_{1-x}N$ compositions, etch rates increased with increase in substrate bias voltage. This increase is due to higher rates of physical sputtering and/or the rate of surface chemical reactions to produce volatile species. Etch rates for GaN and AlN increased from 46 to 497 nm/min and 5 to 263 nm/min, respectively, as the bias voltage increased from −50 to −250 V. An etch rate of 3.5 nm/min was also achieved for GaN at a bias voltage of −7 V. This is the lowest bias value reported to date at which an etch rate for GaN was observed. The same data, when plotted as a function of the fraction of x in $Al_xGa_{1-x}N$, as in Fig. 2(b), showed that no significant change in selectivity between GaN and AlN occurs above −100 V bias values.

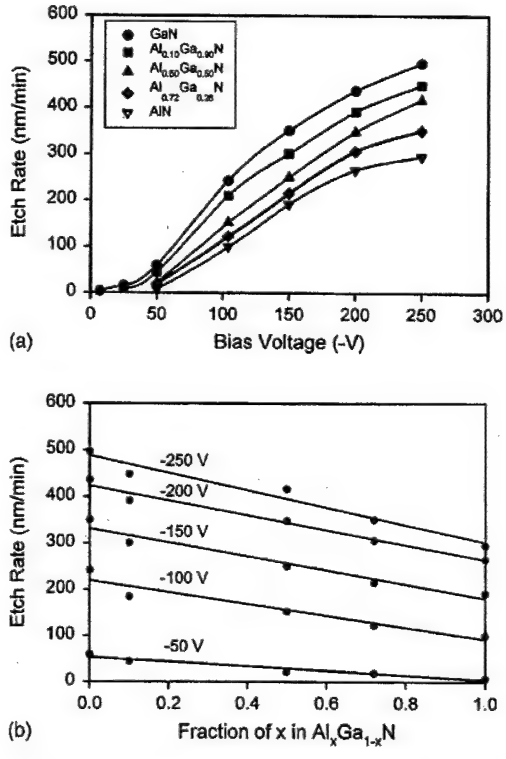

FIG. 2. (a) Etch rate vs bias voltage. (b) Etch rate vs fraction of x in $Al_xGa_{1-x}N$ (ICP coil power=500 W; pressure=5 mT; and gas flow rate =25/5 sccm of Cl_2/Ar).

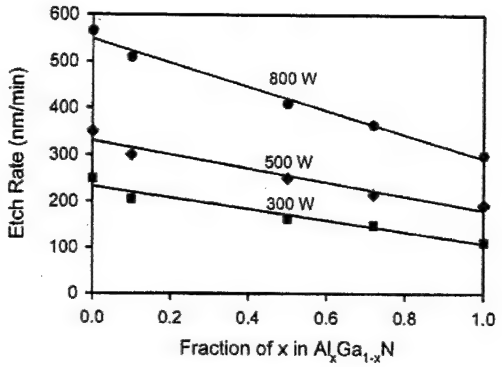

FIG. 3. Etch rate vs fraction of x in $Al_xGa_{1-x}N$ (bias voltage=−150 V; pressure=5 mT; and gas flow rate=25/5 sccm of Cl_2/Ar).

The etch rates were also observed to decrease as the value of x increased from GaN to AlN. This may be attributed to the increase in bond energy of $Al_xGa_{1-x}N$ with an increase in the value of x. This may also be due to some background oxygen present in the chamber which will result in reducing the etch rate of Al-containing samples. However, since our ICP chamber is load locked, the effect of background oxygen on the etch rates should be minimal.[15]

$Al_xGa_{1-x}N$ etch rates as a function of x for ICP coil powers of 300, 500, and 800 W are shown in Fig. 3. Bias voltage and chamber pressure were kept constant at −150 V and 5 mT, respectively. An increase in the ICP coil power increases the density of the plasma in the chamber, and consequently, the density of the ions arriving on the surface of the substrate. Therefore, higher values of ICP coil power at constant voltage values should result in an increase in the chemical component of the etching mechanism. Surface chemical reactions are dependent on the reaction activation energies, which in turn are dependent on bond energies of the material being etched. Since the average bond energy increases as we increase the concentration of Al in $Al_xGa_{1-x}N$, we would expect a higher change in the rage of surface chemical reactions for GaN than AlN, producing a change in the slope of the iso-coil-power etch rate lines as we change the ICP coil power. Etch rates increased from 250 to 566 nm/min and 112 to 300 nm/min for GaN and AlN, respectively, as the ICP coil power was increased from 300 to 800 W.

GaN and $Al_{0.10}Ga_{0.90}N$ etch rates as a function of chamber pressure are shown in Fig. 4. An interaction between the chamber pressure and both the ICP coil power and substrate bias voltage was observed. Keeping the ICP coil power at 500 W, when the bias voltage was increased from −150 to −300 V, the optimum etching pressure to obtain the highest etch rate was observed to increase from 3 to 5 mT as shown in Fig. 4(a). Similarly, keeping the bias voltage value at −300 V, as the ICP coil power was increased from 500 to 700 W the optimum etching pressure was observed to increase from 5 to 7 mT. At higher pressures, the collision frequency of ions that produce neutrals increases, resulting in a decrease in etch rate. However, at higher pressures more ions can be produced by increasing the ICP coil power. Moreover, by also increasing the bias voltage we can in-

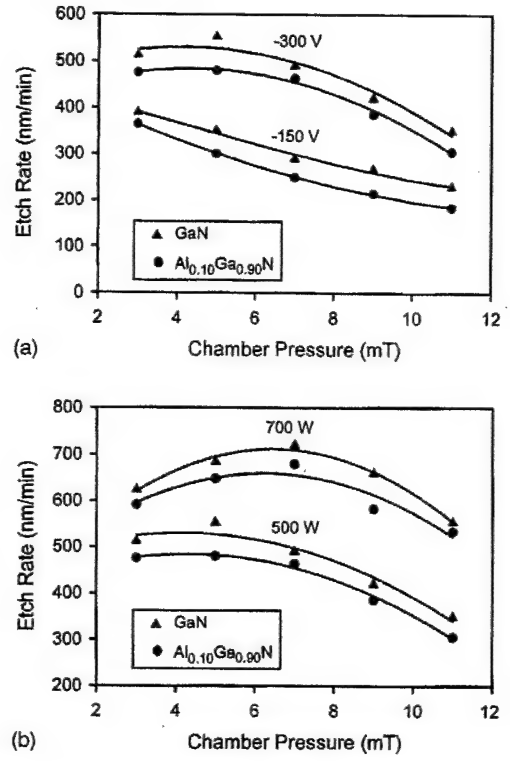

FIG. 4. (a) Etch rate vs chamber pressure for bias voltages of −150 and −300 V (ICP coil power=500 W; pressure=5 mT; and gas flow rate=25/5 sccm of Cl_2/Ar). (b) Etch rate vs chamber pressure for ICP coil powers of 500 and 700 W (bias voltage=−300 V; pressure=5 mT; and gas flow rate=25/5 sccm of Cl_2/Ar).

crease the probability that more ions reach the substrate before they recombine to form neutrals. Therefore, by increasing the ICP coil power and/or the bias voltage, we can overcome the reduction in etch rate due to the increased number of neutrals.

Figure 5 shows etch rates for GaN and $Al_{0.10}Ga_{0.90}N$ as a function of the fraction of Cl_2 in the Cl_2/Ar gas mixture. Bias voltage, ICP coil power, and chamber pressure were kept constant at −150 V, 500 W, and 5 mT, respectively. The etch rate was found to be relatively insensitive, within

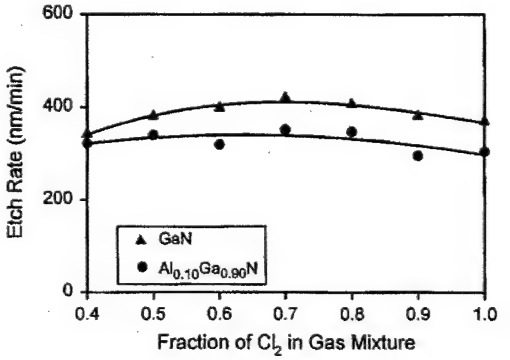

FIG. 5. Etch rate vs gas mixture composition (ICP coil power=500 W; bias voltage=−150 V; pressure=5 mT; and total gas flow rate=30 sccm of Cl_2/Ar).

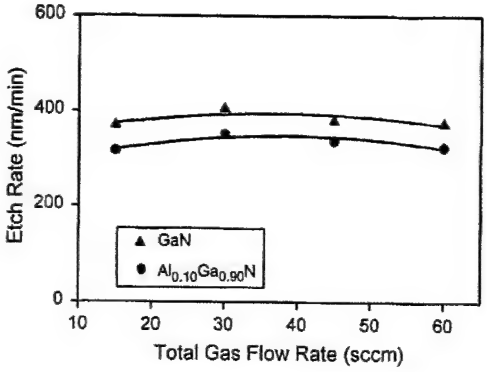

FIG. 6. Etch rate vs gas flow rate (ICP coil power=500 W; bias voltage =−150 V; pressure=5 mT; and gas ratio=70% Cl_2 and 30% Ar).

error uncertainties, to the change in Cl_2 percentage in the Cl_2/Ar gas mixture. Etch rates were also studied as a function of flow rate at −150 V bias, 500 W ICP coil power, 5 mT chamber pressure, and 70% Cl_2 present in the Cl_2/Ar gas mixture. Very little change in etch rates was observed with change in flow rate as shown in Fig. 6.

Auger electron spectroscopy (AES) analysis was performed on etched $Al_{0.22}Ga_{0.78}N$ layers to investigate etch-induced surface stoichiometric changes. The AES spectra of an unetched control sample is shown in Fig. 7(a). Figure 7(b) shows an ICP-RIE etched sample at 800 W ICP coil power and −300 V bias voltage while Fig. 7(c) shows an ICP-RIE etched sample at 300 W ICP coil power and −50 V bias voltage. The chamber pressure was kept at 5 mT and the etching time was 30 s. The surfaces of all samples were cleaned in dilute HF solution before being analyzed. The C

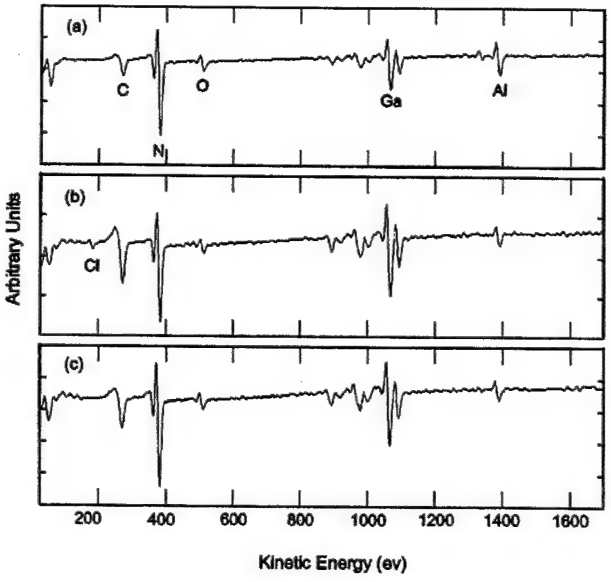

FIG. 7. AES of (a) an unetched $Al_{0.22}Ga_{0.78}N$ sample. (b) $Al_{0.22}Ga_{0.78}N$ sample etched at ICP coil power=800 W; bias voltage=−300 V; pressure=5 mT; and gas flow rate=25/5 sccm of Cl_2/Ar. (c) $Al_{0.22}Ga_{0.78}N$ sample etched at ICP coil power=300 W; bias voltage=−50 V; pressure=5 mT; and gas flow rate=25/5 sccm of Cl_2/Ar.

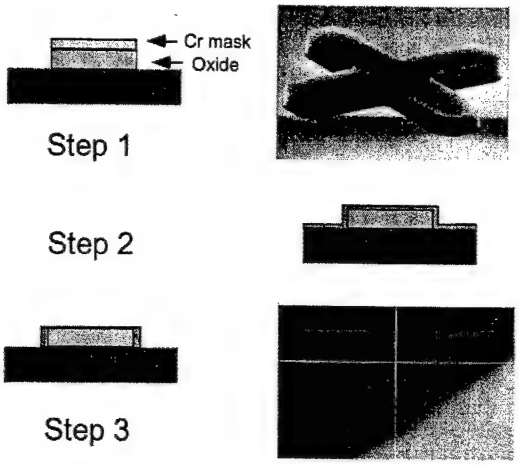

FIG. 8. (a) Oxide masking scheme. Step 1: RIE etch the PECVD Si_xO_y using a Cr mask. Step 2: Remove Cr and redeposit a thin layer of PECVD Si_xO_y. Step 3: RIE etch back the oxide layer.

and O peaks in the various spectra are due to the atmospheric exposure. The Cl in the spectra of the etched sample is from the etchant gas. After HF cleaning, the spectra of the etched surfaces were observed to be identical, independent of the etching condition. Within experimental error, the relative concentration of N, Al, and Ga on the etched samples was observed to be identical to the unetched control sample.

B. Smooth facet formation

Laser facets may require etched depths exceeding a few microns. At the same time, they need to be very smooth and highly anisotropic. Therefore, processes for etching facets require high etch rates to minimize the etching time. They also require low etch selectivity between the various substrate layers so that the etch rate is not significantly affected by any particular layer. At the same time, they require high etch selectivity between the mask and the substrate. A low etch selectivity would require an increase in mask thickness and might result in degradation of the anisotropy and sidewall smoothness of the etched facet. The etch rate study showed that optimization of an etch process to fulfill these requirements requires optimized values for bias voltage, ICP coil power, and chamber pressure. As shown in Fig. 2(a), increasing the bias voltage increases the etch rate. However, higher bias values reduce the etch selectivity between the masking material and the substrate. Increasing the ICP coil power also increases the etch rate at the expense of the etch selectivity between the mask and the substrate. An increase in chamber pressure was observed to degrade the smoothness of the etched facets.

A high-quality facet also requires a high-quality mask (see Fig. 8). Any degradation in the quality of the mask is etched directly into the facet.[16] A Si_xO_y mask was used in this study. The mask was deposited on the GaN/InGaN/AlGaN heterostructure laser material by a PECVD system. A 100-nm-thick Cr mask, patterned on Si_xO_y by lift-off, was used to etch the Si_xO_y. Any edge imperfections present in the Cr mask would get etched into the Si_xO_y during this step. To smooth them out, the Cr was removed and a thin layer of PECVD Si_xO_y was redeposited on top of the etched oxide followed by a RIE blanket etch back. An etched facet using this masking scheme is shown in Fig. 9. The facet was etched at -160 V bias voltage, 500 W ICP coil power, 2 mT chamber pressure with a flow rage of 25 sccm of Cl_2, and 5 sccm of Ar. The roughness of the facet as viewed in a scanning electron microscope was less than 20 nm. The sidewall angle with respect to the surface normal was less than 1°.

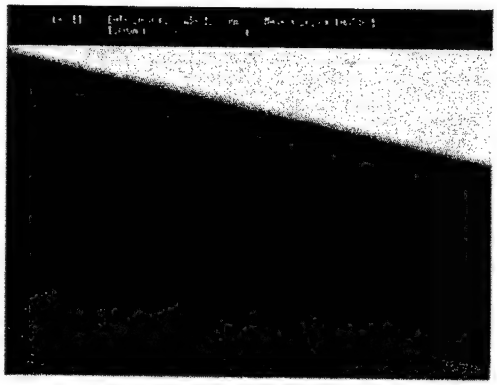

FIG. 9. Etched facet in GaN/InGaN/AlGaN heterostructure laser material.

IV. CONCLUSIONS

In summary, etch rates of $Al_xGa_{1-x}N$ over the entire compositional range were investigated using inductively coupled plasma reactive ion etching in Cl_2/Ar gas mixtures. Etch rates were found to increase with bias voltage and ICP coil power. Etch rates were also observed to decrease with an increase in Al composition. Optimum chamber pressure for etch rates was found to be dependent on both the ICP coil power and bias voltage. Very little change in etch rate was observed as the gas mixture or the total gas flow rate was changed under the etching conditions being investigated. Auger electron spectroscopy analysis showed that the composition of the etched surfaces was identical, independent of the etching conditions. High-quality etched facets in GaN/InGaN/AlGaN heterostructure laser material were also successfully fabricated.

ACKNOWLEDGMENTS

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Rapid evaluation of dislocation densities in *n*-type GaN films using photoenhanced wet etching

C. Youtsey[a)]
Department of Electrical and Computer Engineering and Microelectronics Laboratory, University of Illinois, Urbana, Illinois 61801

L. T. Romano
Xerox Palo Alto Research Center, Palo Alto, California 94306

R. J. Molnar
Massachusetts Institute of Technology, Lincoln Laboratory, Lexington, Massachusetts 02173

I. Adesida
Department of Electrical and Computer Engineering and Microelectronics Laboratory, University of Illinois, Urbana, Illinois 61801

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We describe a technique based on photoelectrochemical wet etching that enables efficient and accurate evaluation of dislocation densities in *n*-type GaN films. The etching process utilizes dilute aqueous KOH solutions and Hg arc lamp illumination to produce etched GaN "whiskers" by selectively etching away material around threading dislocations. The etched whiskers, each corresponding to a single threading dislocation, can be effectively imaged by plan-view scanning electron microscopy. The distribution and density of dislocations are then readily observed over very large sample areas. Transmission electron microscope and atomic force microscope studies of the GaN samples confirm the accuracy of the dislocation density obtained by the wet etching. © *1999 American Institute of Physics.* [S0003-6951(99)04416-2]

Epitaxial GaN films grown on sapphire or SiC typically have very high dislocation densities in the range of $10^8-10^{10}/\text{cm}^2$. The technique of lateral epitaxial overgrowth (LEO) of GaN has recently enabled significant reductions in dislocation density, with consequent improvements in material optical and electrical characteristics as well as device performance.[1–3] The ability to rapidly assess improvements in material quality that result from new growth techniques and conditions is essential to the material development cycle. Presently, transmission electron microscopy (TEM) is the most effective means of observing dislocations in GaN films. However, the principal disadvantage of TEM is that it requires extensive and skillful sample preparation, especially for GaN and related compounds. Nanometer-scale pits have been observed by atomic force microscopy (AFM) on very smooth GaN surfaces. These pits have been correlated with the surface termination of dislocations.[4] The effectiveness of this method for measuring dislocation densities, however, depends upon the smoothness of the nitride surface and the size of the surface pits. Frequently, pits associated with edge-type dislocations are very small and are less readily observed.

We have recently described a photoelectrochemical (PEC) wet etching process that produces highly anisotropic "whiskers" in *n*-type GaN films by selectively etching away material *between* threading dislocations.[5] The etched whiskers are typically between 10 and 50 nm in diameter and can be up to 1 μm or more in height. TEM analysis of the etched whiskers has confirmed that they contain threading dislocations at their centers.[5] Whisker formation was associated with both edge and mixed character dislocations. The mechanism for the etching selectivity is believed to arise from electrical activity at the dislocations, which influences the localized concentrations of photogenerated holes at the dislocations.[5]

In this letter, we describe an effective process for rapidly and accurately assessing dislocation densities in *n*-type GaN films using PEC etching. The PEC etch process is carried out with a relatively simple apparatus, and the etched whiskers can be readily observed by scanning electron microscopy (SEM) or AFM. Plan-view TEM analysis confirmed a close correlation between the actual dislocation density in the films and the density of etched whiskers. In addition, we have observed a one-to-one correspondence between the nanometer surface pits identified (before etching) by AFM, and the whiskers that subsequently formed by etching in the *identical* region of the GaN sample.

Two different sets of GaN samples were studied in this work. The first were unintentionally doped ($n\sim1\times10^{17}$) GaN films grown on sapphire substrates by hydride vapor phase epitaxy (HVPE) with a thickness of 70 μm. The second set of samples consisted of 2-μm-thick, Si-doped ($n\sim1\times10^{18}$) GaN films that were grown by metalorganic chemical vapor deposition (MOCVD) on SiC substrates. Cross-sectional TEM analysis of the MOCVD GaN films on SiC showed a dislocation density in the low-10^9 cm^{-2} range. Plan-view TEM studies of the HVPE films previously indicated a very low defect density in the range of mid-10^7–mid-10^8 cm^{-2}.[6]

The experimental setup used for the etching is described

a)Electronic mail: cyoutsey@nanovation.com

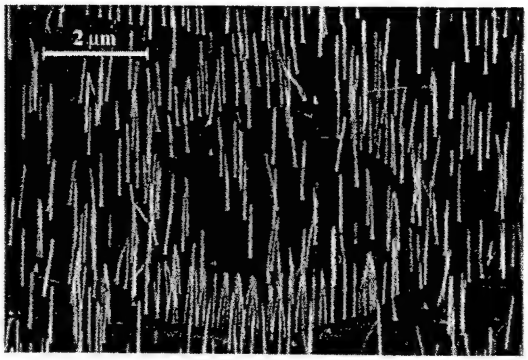

FIG. 1. SEM micrograph of whiskers produced by selective etching of dislocations in a HVPE GaN film. The ring-like structure is suggestive of a misoriented grain in the nitride film.

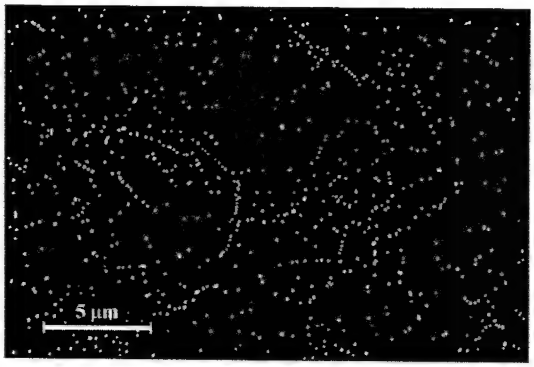

FIG. 2. Low-magnification plan-view scanning electron micrograph of etched whiskers in a HVPE GaN film. The etched whiskers provide a useful map of the distribution of dislocations in the nitride film. The dislocation density is estimated from this image to be 2.1×10^8 cm^{-2}.

in detail elsewhere.[7] The GaN samples were illuminated during the etching by a 350 W Hg arc lamp with a typical intensity of 25 mW/cm^2 at 365 nm. The electrolyte consisted of dilute aqueous solutions of KOH with concentrations in the range of 0.002–0.006 M. The solutions were magnetically stirred during the etching. The etch rate of the GaN under these conditions was approximately 25 nm/min.

Whisker formation occurred only under very specific process conditions that produced a high etch selectivity at the dislocations. We have previously reported whisker formation in narrow window of solution concentration (0.01–0.04 M KOH) for unstirred solutions.[5] Stirring the solution during etching provided more controllable process conditions by enabling whisker formation over a wider range of solution concentration (compared to unstirred solutions). When using stirred solutions, selective etching occurred for concentrations of 0.001–0.01 M KOH. Note that these solutions are significantly more dilute than for the unstirred case. The solution concentrations that enable the selective etching of dislocations appear to correspond to moderately diffusion-limited etching conditions. Decreasing the solution concentration further resulted in a strongly diffusion-limited etch process and a smooth etched surface morphology free of whiskers.[8]

The SEM micrograph shown in Fig. 1 demonstrates the etched whiskers produced by the selective PEC etching process. The HVPE GaN sample shown in this image was etched for 45 min in a stirred 0.004 M KOH solution. The etched whiskers are approximately 50 nm thick and 1 μm tall. Note that the 1 μm whisker height corresponds to the *removal* of 1 μm of GaN material around the threading dislocations. Some of the threading dislocations are due to rotational misalignments between adjacent islands during the early stages of growth.[6,9–11] These have been found by TEM experiments to be edge dislocations with burgers vector $\mathbf{b} = 1/3\langle 1120\rangle$.[9–11] In some regions of the sample, as indicated in Fig. 1, the distribution of whiskers is seen to form a "ring-like" structure, suggestive of a cell boundary. The diameter of the ring, in this case, is about 4 μm and the spacing D of the dislocations within the ring is approximately 0.1 μm. Using the simple relationship for low angle grain boundaries, $\theta = \mathbf{b}/D$,[12] the misorientation angle θ, for burgers vector $\mathbf{b} = 0.319$ nm, can be determined. The value was found to correspond to a "grain" that is misoriented with respect to the matrix by 9.8 min. This is comparable to the width of the x-ray diffraction rocking curve found for the (102) asymmetric reflection,[6] which is associated with edge dislocations.[13]

Plan-view SEM is an effective technique to observe the population of etched whiskers over very large sample areas. The whiskers are sharp surface discontinuities and provide high contrast against the smooth background surface. Figure 2 shows a 15×25 μm^2 plan-view SEM image of an etched HVPE sample. The image brightness and contrast have been optimized so that the etched whiskers appear as bright points against a dark background, imparting on Fig. 2 a star-map appearance. The use of plan-view TEM to observe dislocations in GaN is effective only for substantially smaller areas than seen in Fig. 2. The ability to survey large sample areas is especially critical for samples with low dislocation densities. (A dislocation density of 10^6 cm^{-2} corresponds to one dislocation in 100 μm^2.) The dislocation density in Fig. 2 is estimated at 2.1×10^8 cm^{-2}.

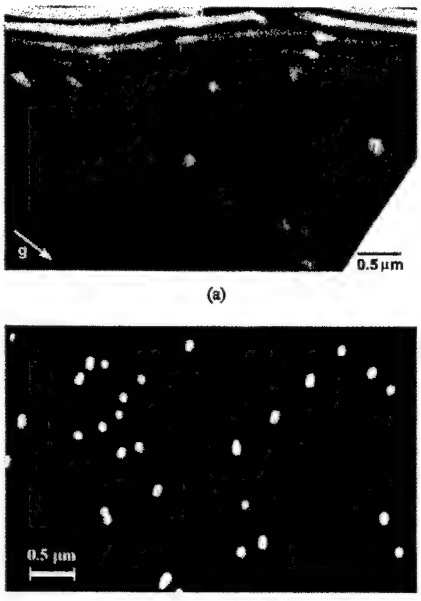

FIG. 3. (a) Plan-view TEM micrograph of HVPE GaN film. The dislocation density is estimated from the TEM image to be 1.8×10^8 cm^{-2}. (b) A subsection of the dislocation map from Fig. 2, shown at a comparable magnification to the TEM image in (a).

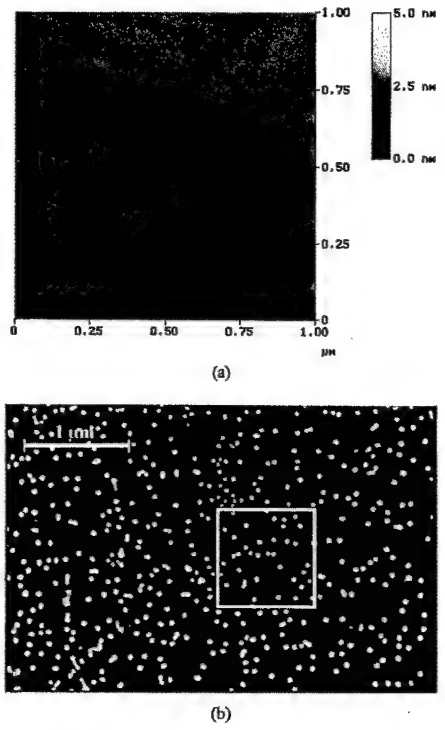

FIG. 4. (a) AFM image of *unetched* MOCVD GaN film. The high density of nanometer-scale surface pits are associated with the surface termination of threading dislocations. (b) Plan-view SEM micrograph of etched whiskers produced in the *identical* surface region of the GaN sample shown in Fig. 4(a). The white box indicates the 1×1 μm^2 area surveyed by AFM. A one-to-one correspondence exists between the etched whiskers and the surface pits seen before etching by AFM. The dislocation density is estimated at 3.6×10^{-9} cm^{-2}.

It is important to verify that the PEC etch technique and TEM produce similar estimates of dislocation density in GaN films. Figure 3(a) shows a plan-view TEM image of the HVPE film. The TEM image indicates a dislocation density of approximately 1.8×10^{8} cm^{-2}, which is similar to the etched whisker density shown in Fig. 2. For comparison, Fig. 3(b) shows a region of Fig. 2 that has been enlarged to a similar magnification as the TEM image in Fig. 3(a).

AFM surface scans of GaN epitaxial films frequently reveal nanometer-scale surface "pits," which have been previously attributed to the surface termination of threading dislocations.[4] On very smooth GaN films, these pits are generally observed to be positioned at surface step terminations, which suggests that the pits are correlated with dislocations of pure screw or mixed character. High quality AFM can also sometimes be used to observe smaller pits that do not occur at atomic terraces, which may be associated with pure edge dislocations.[4] Since the AFM technique is nondestructive, we conducted an AFM study of a particular GaN surface, and then subsequently etched the GaN sample and observed the resulting etch characteristics on the same region of the sample. Metal alignment marks were patterned onto the sample to facilitate relocating the identical area of the sample with submicron reproducibility.

Figure 4(a) shows a 1×1 μm^2 AFM surface scan of an unetched GaN film grown by MOCVD on SiC. The root mean square (rms) roughness of the unetched film was approximately 0.3 nm. A high density of surface pits is observed on the unetched surface, as described above. The GaN sample was then etched using a stirred 0.004 K KOH solution for 15 min. A plan-view SEM image of exactly the same area of the sample after etching is shown in Fig. 4(b). The original 1×1 μm^2 area imaged by AFM in Fig. 4(a) is identified in Fig. 4(b) with a white box. The nanometer pits observed by AFM closely map onto the whiskers produced by the PEC etching. The dislocation density for the MOCVD samples in Fig. 4 is estimated at 3.6×10^{-9} cm^{-2}.

In summary, a technique has been developed for revealing and estimating dislocations in *n*-type GaN films through photoelectrochemical wet etching. The etching process produces highly anisotropic whiskers by selectively removing material between threading dislocations. The etched whiskers provide an accurate map of both edge and mixed character dislocations in the GaN material. A close correspondence between the whiskers and threading dislocations has been confirmed through TEM and AFM analysis.

G. Bulman of Cree Research, Inc. is acknowledged for providing MOCVD-grown samples used in this study. The authors are grateful to P. Fay and K. Youtsey for their insightful conversations. This research was supported at the University of Illinois by NSF Grant No. ECS 95-21671 and DARPA Grant No. F19628-96-C-0066, and at Xerox PARC by DARPA Grant No. MDA972-96-3-0014.

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for the circuit in Fig. 2*b*, giving improvements of a factor of 1.7 and 2.6, respectively, over the typical one-octave tuning range obtained from the *npn*-only f_T-integrator. At nominal conditions in both circuits, the phase errors at fU were less than 3.8° (for DC gains of 40dB). In an f_T integrator-based resonator design, this phase error is not usually a significant problem since it can be mitigated by the frequency/DC-gain control circuit embedded within the integrator [2]. Fig. 3 illustrates the frequency response close to the tuning extremes of the circuit in Fig. 2*b*. Total output harmonic distortion of < –40dB for an input at f_U is achieved over the entire tuning range with the output current swing up to 50% modulation index (peak) in both integrators. The test frequency at the unity gain of the integrator was chosen because it would typically be the centre frequency of the resonator in which the f_T integrators operate. Also, at such frequencies, parasitic capacitances become significant, and simulations suggest that better linearity can be achieved at frequencies below the f_U.

f_T-integrators in CMOS technology: In an *n*-well CMOS process where the well is used to form the *n*-type base of the bipolar junction transistor (BJT), there are two types of bipolar transistor readily available without additional process steps, namely substrate or vertical *pnp* (whose collector is always tied to the substrate) and lateral *pnp*. It is therefore conceptually straightforward and attractive to implement f_T integrators using the lateral *pnp*. As the f_T integration technique requires no physical linear capacitors, the scheme is entirely compatible with standard digital CMOS technologies. With a 0.6μm CMOS technology, an f_T integrator with a structure similar to that in Fig. 1 was simulated using only lateral *pnp* transistors ($\beta_0 \simeq 12$ and $f_T \simeq 170$MHz with nominal biasing collector current of 30μA). Simulation results show that the circuit is tunable from 50MHz to 110MHz with total harmonic distortion of < –46dB over the entire tuning range (for an input signal at f_U and with an output current swing up to 50% modulation depth). These results suggest that lateral *pnp* devices may have a role to play in continuous time signal processing using digital CMOS technologies.

Conclusions: The implementation of f_T integrators using commonly available lateral *pnp* transistors in standard BiCMOS and CMOS processes has been demonstrated. Owing to the relatively large-base transit time and low nominal biasing current of these lateral *pnp* devices, the simulated integrators possess significantly improved tuning capability with less power consumption compared to the previous *npn*-only circuits. It is expected that this improvement will enable the design of f_T-integrator based resonators, filters and oscillators with wider tuning range, and reduced power and chip area. A resonator based on the aforementioned f_T-integrators is being tested and will be presented elsewhere.

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P. Khumsat and A.J. Payne (*Department of Electrical and Electronic Engineering, Imperial College of Science, Technology and Medicine, London SW7 2BT, United Kingdom*)

E-mail: p.khumsat@ic.ac.uk

A. Worapishet (*Department of Telecommunication Engineering, Mahanakorn University of Technology, Bangkok 10530, Thailand*)

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Gate recessing of GaN MESFETs using photoelectrochemical wet etching

A.T. Ping, D. Selvanathan, C. Youtsey, E. Piner, J. Redwing and I. Adesida

For the first time GaN-based MESFETs which have been recessed using a wet etching process are presented. Photoelectrochemical etching was used to recess openings through the heavily-doped *n*-GaN cap and into the *n*-GaN channel. The DC and RF characteristics of recessed-gate GaN MESFETs are presented.

Introduction: The performance of field-effect transistors based on the group-III nitrides has been impressive and demonstrates the potential of these materials for high-power and high-temperature applications [1, 2]. However, significant improvements in the device performance can still be obtained through optimisation of the drain-source ohmic contacts. One method for improving the ohmic contact resistance involves gate recessing a heavily-doped cap layer, which is carried out extensively in other III-V material systems. However, the inability to chemically wet etch the nitrides has made it difficult to apply gate recessing techniques to the nitride system. A wet etching process called photoelectrochemical (PEC) etching has recently been demonstrated to be a viable technique in etching *n*-type GaN [3, 4]. This technique is capable of producing high etch rates, highly anisotropic etch structures, and very smooth surfaces depending on the electrolyte concentration and light intensity [4, 5]. This technique also offers damage-free etching since photons and not ions are used to initiate the etching process. These etching attributes, i.e. smooth etch surfaces and damage-free etching, are very attractive and necessary for fabricating recessed-gate devices. In this Letter, we present for the first time the successful application of PEC etching in the gate recessing of GaN-based FETs.

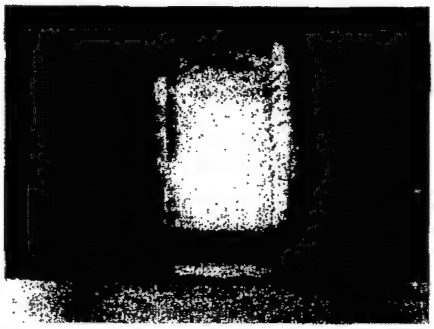

Fig. 1 *SEM photograph of 1μm wide opening recessed using PEC*

Device fabrication: The layer used in the study presented in this Letter was grown on sapphire substrates by metal organic vapour epitaxy (MOVPE). The epilayer consisted of an AlN buffer, 2μm of insulating GaN, a 2000Å lightly-doped *n*-GaN channel (~2×10^{17}cm^{-3}), and a 400Å highly-doped (>5×10^{18}cm^{3}) GaN cap. Mesa isolation was achieved using chemically assisted ion beam etching. The drain-source ohmic contacts consisted of rapid-thermally annealed Ti/Al/Ti/Au. The formation of the recessed Schottky gate was performed using a two step lithography process. First, electron-beam lithography was used to pattern 1μm wide openings centred within the drain-source region. The n^+ GaN cap was then recessed away using PEC under conditions described by Youtsey *et al.* [5]. A second electron-beam lithography step was used to pattern mushroom-shaped 0.25μm gates within the 1μm wide recess openings. The Schottky gate consisted of Ni/Au. The total device width was 100μm. Fig. 1 shows an SEM photograph of a 1μm wide recessed opening which was etched by the PEC process. Note that the etched surface is smooth. An SEM photograph of a completed recessed-gate GaN MESFET is shown in Fig. 2.

Device performance: Fig. 3*a* and *b* shows the common-source I_{DS}–V_{DS} and transfer characteristics, respectively, for a typical 0.25μm gate-length recessed-gate GaN MESFET. The drain-source

spacing was nominally 3μm. A peak I_{DS} of 354mA/mm was measured. The transfer characteristics show good pinch-off characteristics with a peak extrinsic transconductance ($g_{m,ext}$) of 33mS/mm at a gate bias of −4.5V. The output conductance, measured at the bias for peak $g_{m,ext}$, was 11.4mS/mm. The maximum achievable

Fig. 2 *SEM side view of completed recessed-gate GaN MESFET with 1μm recess opening and 0.25μm gate*

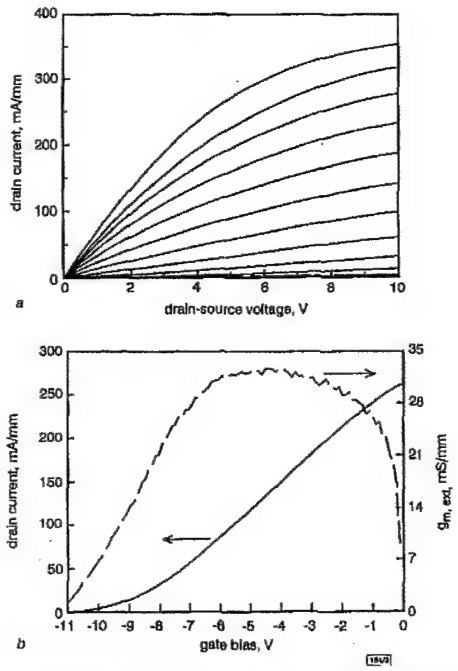

Fig. 3 *Common-source I_{DS}–V_{DS} characteristics where gate potential was swept from 0 to −10V in −1V increments, and transfer characteristics with drain-source bias fixed at 6V*

a Common-source characteristics
b Transfer characteristics

gain (g_m/g_o) is thus 2.9 for these devices. The threshold voltage was −8.6V and was found from the V_{GS} intercept of the extrapolation of a tangent from the I_D curve at the point of maximum $g_{m,ext}$. This value is very high and indicates that a significant portion of the channel was not recessed away by the PEC. The gate-to-drain I-V characteristics (not shown) were well-behaved with a forward turn-on voltage of 0.9V. The reverse-bias breakdown exceeded 20V with a gate leakage current of ~60μA at −20V. These characteristics showed that the PEC was successful in removing the heavily-doped *n*-GaN cap material from under the gate metal contact.

The small-signal characteristics were measured from 1 to 35GHz using an HP8510 network analyser. The current-gain cut-off frequency (f_T) and maximum frequency of oscillation (f_{max}) were extrapolated from $|h_{21}|$ and G_{Amax} data, respectively, at −20dB/decade. A peak f_T of 12GHz and an f_{max} of 23GHz were measured at drain and gate biases of 8 and −2.6V, respectively.

To the best of the authors' knowledge, we have demonstrated for the first time GaN-based FETs which were recessed using a wet etching process. The recessed areas tended to be smooth to slightly rough. The devices had an I_{DS} of 354 mA/mm, a $g_{m,ext}$ of 33mS/mm, an f_T of 12GHz, and an f_{max} of 23GHz. Further advances such as double-recess gate technology are currently being developed for the fabrication of GaN-based MESFETs and HEMTs.

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A.T. Ping, D. Selvanathan, C. Youtsey, and I. Adesida (*Microelectronics Laboratory and Department of Electrical and Computer Engineering, University of Illinois, Urbana, IL 61801, USA*)

E. Piner and J. Redwing (*ATMI/Epitronics, Phoenix, AZ 85027, USA*)

C. Youtsey: Present address: Nanovation Technologies, Inc., Evanston, IL 60602, USA

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Impact of nonlinear drain resistance in bias-stressed InAlAs/InGaAs HEMTs

T. Suemitsu, H. Yokoyama and Y. Ishii

A study of the degradation of drain current under bias and temperature stress is presented for InP-based InAlAs/InGaAs HEMTs. Nonlinear drain resistance has been found to play an important role in the degradation. The decrease in the drain current is caused by the rapid increase in the drain resistance. The result suggests that the carrier density, which is originally sufficient to keep the resistance low and linear, decreases in the drain ohmic region.

InP-based high electron mobility transistors (HEMTs) are the most promising devices for high-speed applications such as optical communication systems and high-frequency ICs. In state-of-the-art technology a current gain cutoff frequency of 350GHz with a gate length of 30nm has been achieved [1]. Long-term reliability is an important issue for device application. The decrease in the drain current (I_d) is one of the major problems with respect to reliability [2]. Although a positive shift in the threshold voltage (V_{th}) decreases I_d, a decrease in I_d is also observed in HEMTs without a shift in V_{th} [2]. The increase in the drain resistance is a common failure mode observed in InP-based HEMTs [2 – 4]. However, a simple change in the drain resistance does not significantly affect I_d when the HEMT is operated in the saturation region. No detailed model has been reported for this degradation.

Low resistance Ti/Pt/Au ohmic contacts to *p*-type GaN

L. Zhou,[a] W. Lanford, A. T. Ping, and I. Adesida
Department of Electrical and Computer Engineering and Microelectronics Laboratory, University of Illinois, Urbana, Illinois 61801

J. W. Yang and A. Khan
Department of Electrical and Computer Engineering, University of South Carolina, Columbia, South Carolina 29208

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Electrical properties of Ti (15 nm)/Pt (50 nm)/Au (80 nm) contacts on moderately doped *p*-GaN ($N_A = 3.0\times10^{17}\,\mathrm{cm}^{-3}$) are reported. Linear current–voltage characteristics were observed after annealing the contacts for 1 min at temperatures above 700 °C. The best ohmic contacts were obtained after annealing in a N_2 ambient at 800 °C for 2 min. These contacts exhibited a specific contact resistance R_c of $4.2\times10^{-5}\,\Omega\,\mathrm{cm}^2$ and contact resistivity ρ_c of 21 Ω mm. Possible mechanisms for the lower contact resistivity of Ti/Pt/Au contacts are discussed. The processing for the Ti/Pt/Au ohmic contacts is compatible with routine fabrication steps for GaN devices. © *2000 American Institute of Physics.* [S0003-6951(00)03723-2]

The realization of excellent ohmic contacts on *p*-type gallium nitride (GaN) remains a key hurdle in the development of optoelectronic devices based on this material system. Obtaining low resistance ohmic contacts for the *p*-type GaN has been an enormous challenge due to a large 3.4 eV band gap, a deep acceptor level of 215 meV for the commonly used Mg dopant, and the difficulty of obtaining dopant levels as high as $10^{18}\,\mathrm{cm}^{-3}$.[1] Metal–semiconductor interface studies have revealed that surface contamination is directly correlated with increased metal–semiconductor barrier heights for metal contacts on *p*-GaN.[2,3] These studies provide strong evidence that the Fermi level is not pinned at the metal/*p*-GaN interface as previously believed.[4] Unfortunately, attempts at using metals with high work functions to reduce contact resistances on *p*-GaN have not been very successful. So far, only two ohmic metallization processes have been reported on moderately doped *p*-GaN that have achieved specific contact resistances R_c less than $10^{-4}\,\Omega\,\mathrm{cm}^2$.[5,6] One of these methods uses Ta/Ti bilayer contacts and requires a postdeposition anneal of 20 min at 800 °C to achieve $R_c = 3\times10^{-5}\,\Omega\,\mathrm{cm}^2$ on *p*-GaN doped at $7\times10^{17}\,\mathrm{cm}^{-3}$. However, this contact is unstable in air.[5,7] Another low-resistance contact scheme, which is capable of achieving a R_c as low as $4\times10^{-6}\,\Omega\,\mathrm{cm}^2$, requires deliberate oxidation of the Ni/Au contacts at 500 °C for 10 min.[6,8,9] In both cases, the reduction of the contact resistance were attributed to reactivation of the Mg dopant by disrupting the bonding in the Mg–H complexes.

In this letter, we report low-resistance ohmic contacts achieved using Ti/Pt/Au metallizations on *p*-GaN. A thin (~15 nm) layer of Ti was first deposited on *p*-GaN. Titanium was selected because it has proven effective in reducing surface contaminations when incorporated in ohmic contacts on *n*-type GaN.[10,11] The second, thicker layer is Pt, chosen primarily for its high work function (5.65 eV). Finally, a thick Au capping layer was used to protect the metallization during subsequent processing. Ti/Pt/Au ohmic contacts have been studied before for other compound semiconductors, such as *n*-type GaAs and *p*-type InGaP.[12,13] Ti/Pt/Au were also candidates for thermally stable contacts on degenerately doped *n*-type InN and $In_xGa_{1-x}N$.[14,15] To our knowledge, there is no published study on the use of Ti/Pt/Au as *p*-GaN ohmic contact metallization.

The *p*-GaN film used in this study was grown by metal-organic chemical vapor deposition on sapphire substrates. An undoped GaN layer with a thickness of 3 μm was grown, followed by the growth of 0.3 μm thick *p*-type GaN doped with Mg. A dopant activation anneal was carried out at 800 °C for 1 min. A bulk carrier concentration of $\sim2.5\times10^{17}\,\mathrm{cm}^{-3}$ and a mobility of $9\,\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$ were obtained from room temperature Hall measurements. Contact resistances were determined using the linear transfer length method (TLM). The active regions used for the TLM measurements were defined by reactive ion etching. Rectangular pads were then patterned on these electrically isolated mesas. Prior to metal evaporation, the surfaces were cleaned in O_2 plasma, followed by dips in a dilute HCl:H_2O(1:2) solution and blown dry in N_2. Electron beam evaporation was used to deposit Ti (15 nm) and Pt (50 nm), while thermal evaporation was used to deposit the Au (80 nm) capping layer. Postdeposition heat treatment was carried out while flowing N_2 at 1 atm in a rapid thermal annealing system. The current–voltage (I–V) and TLM characteristics of the contacts were measured using a four-probe arrangement at room temperature. For accurate R_c determination, actual pad spacings were determined using scanning electron microscopy after pad fabrication.

Figure 1 illustrates the I–V characteristics of the as-deposited and the heat-treated contacts, measured between ohmic pads with a spacing of 3 μm. The contacts are rectifying as deposited, and remain rectifying after annealing at 500 or 600 °C for 1 min. The linearity of the I–V curves improved, however, with higher annealing temperatures. The

[a]Author to whom correspondence should be addressed; electronic mail: lingzhou@uiuc.edu

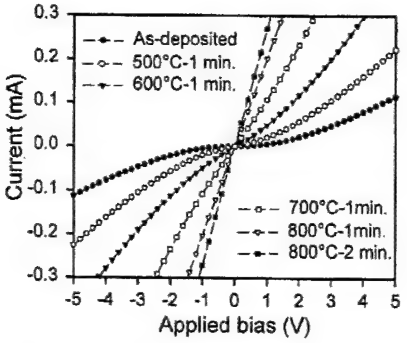

FIG. 1. The $I-V$ characteristics of Ti/Pt/Au contacts on p-GaN before and after heat treatments, measured over ohmic pads with a spacing of 3 μm.

$I-V$ characteristics become linear after annealing at 800 °C, the highest temperature used in this study. Annealing for 2 min at 800 °C showed further but slight improvement of the $I-V$ characteristics. A total resistance R_T versus pad spacing plot is shown in Fig. 2. The slope of R_T versus pad spacing decreased slightly with increasing annealing temperature until 700 °C, then there is an abrupt reduction in slope from 700 to 800 °C. This reduction corresponds to a factor of 3 decrease in the semiconductor sheet resistance R_S, which translates to an increase in the hole concentration by a similar factor. The lowest R_C and contact resistance ρ_c obtained are $4.2\times10^{-5}\,\Omega\,\mathrm{cm}^2$ and 21 Ω mm, respectively, for contacts annealed at 800 °C for 2 min.

It is widely believed that Ti reacts with GaN to form TiN during heat treatment in the Ti/Al contact for n-GaN. [1,16] This reaction creates a thin region rich in N vacancies and becomes, in effect, a heavily doped n-type region. Ti/Al contact resistance is therefore reduced through enhanced tunneling. Such a view has, however, been called into question in several recent studies.[10,17] In any case, if Ti indeed induces a high concentration of N vacancies in the p-GaN samples, then the p-type doping will consequently be heavily compensated, and may even lead to the formation of $p-n$ junctions. This would result in worse ohmic characteristics for Ti/Pt/Au contacts compared to that of Pt or Pt/Au contacts. The fact that Ti/Pt/Au contacts are considerably better than either Pt or Pt/Au contacts reported by other workers[4,18] suggest that a significant generation of N vacancies did not occur during this process. Kim *et al.* have recently demonstrated a $R_c = 1.4\times10^{-4}\,\Omega\,\mathrm{cm}^2$ using a Pt monolayer contact after a

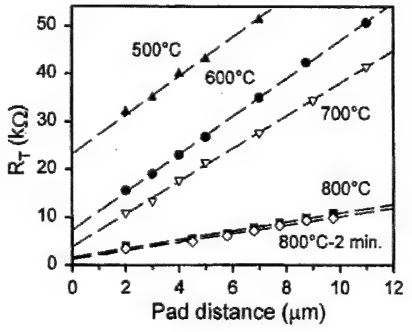

FIG. 2. Plot of the measured total resistance against the contact pad spacing for Ti/Pt/Au contacts. The dotted lines are least square linear fits to the different data sets. Unless otherwise stated, all anneals were carried out for 1 min.

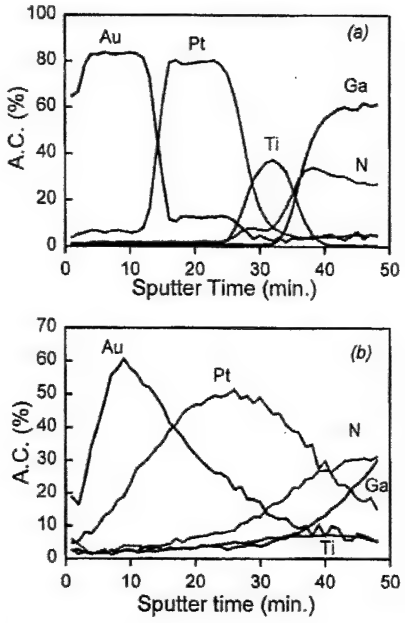

FIG. 3. (a) AES depth profile for the as-deposited Ti(15 nm)/Pt (50 nm)/Au (80 nm) contact. (b) AES depth profile after the contact was annealed at 800 °C for 2 min.

boiling aqua regia surface treatment on p-GaN.[19] Their result suggests that the surface contamination or oxide layer was indeed responsible for the high resistivities of earlier Pt contacts. This result indirectly supports the view that Ti used in the present work is also quite effective in either reducing or gettering surface oxides on p-GaN.

In their study of Ta/Ti contacts to p-GaN,[6,7] Suzuki *et al.* selected Ti and Ta because those metals have lower hydride formation enthalpies compared to that of Mg. A factor of 2–3 increase in hole concentration was measured when the contacts were annealed at 800 °C, numerically very close to our findings as discussed earlier. Therefore, some other resistance-reducing mechanisms may be operating during 800 °C anneals. As well as having the highest work function of all metals, Pt also strongly absorbs hydrogen.[20] One explanation for the aforementioned R_S reduction is that Pt came into contact with GaN after annealing at 800 °C. Figure 3(a) shows the Auger electron spectroscopy (AES) depth profile of as-deposited metals, and Fig. 3(b) shows that significant mixing have occurred for both Ti and Pt with GaN after annealing for 2 min at 800 °C. However, depth profile results (not shown here) also reveal that Pt diffused into GaN at annealing temperatures as low as 500 °C, because the Ti layer used in this study was very thin (15 nm). Therefore, the contact of Pt with p-GaN should be ruled out as the direct cause for the abrupt reduction of R_S at 800 °C. Further experiments are needed to ascertain the exact mechanism(s).

In summary, the Ti/Pt/Au metallization scheme has demonstrated a R_c as low as $4.2\times10^{-5}\,\Omega\,\mathrm{cm}^2$ on moderately doped p-type GaN, and consistently outperforms the conventional Ni/Au contacts on p-GaN. The process used in obtaining this low contact resistance is compatible with routine device fabrication steps. No annealing in oxygen or aqua regia preclean is required. This demonstrates that Ti is effective in neutralizing the effects of contamination/oxide layer on the p-GaN surface. An abrupt decrease in R_S is observed

when annealing at 800 °C. The precise mechanism for this improvement is unclear, although it may be related to the reactivation of Mg dopants, out diffusion of hydrogen, and retention of hydrogen in the Pt layer.

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The LER of mask biasing isolated lines was also investigated using NEB22. By controlling the exposure dose, 100nm isolated lines with the designed widths of 40–120nm were delineated. Fig. 2 shows the SEM photographs of the mask biased lines. The larger biased pattern with the smaller designed width shows smoother line edges. Fig. 3 shows the LER of the 100nm isolated line with mask biasing against 1/slope of the beam profiles calculated for the mask biasing isolated lines. The beam profiles and the slope are defined by the following equations:

$$f(\sigma_{TTL}, x) = \frac{D}{\sigma_{TTL}\sqrt{\pi}} \int_0^W \exp\left(\frac{-(x-t)^2}{\sigma_{TTL}^2}\right) dt \quad (1)$$

$$slope(\sigma_{TTL}) = \left.\frac{\partial f}{\partial x}\right|_{f=threshold\ level} \quad (2)$$

where σ_{TTL}, W, and D represent the beam blur, the designed width and a standardised exposure dose, respectively. The narrower designed width caused the steeper slope. The results indicate that a smaller LER is derived from a steeper slope, which implies that reducing the beam blur results in a decrease in LER because the slope increases with decreasing beam blur. That is, the RL is determined by the beam blur because the RL is proportional to the LER, as shown in Fig. 1.

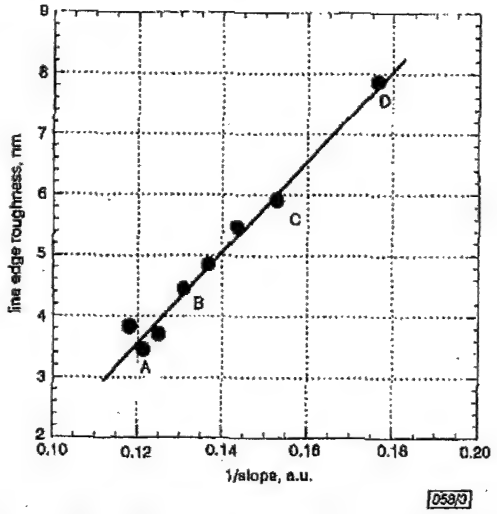

Fig. 3 *Line edge roughness of the 100nm isolated line with mask biasing against 1/slope of beam profile*

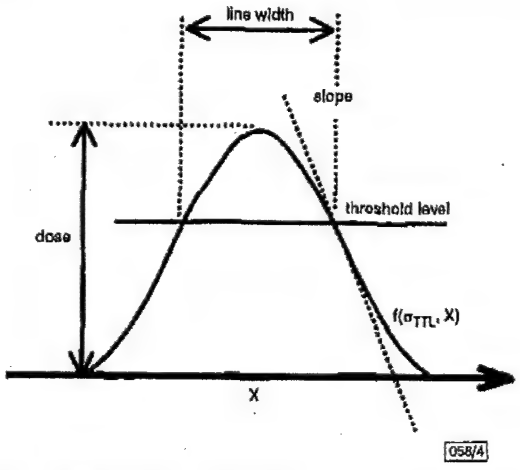

Fig. 4 *Schematic diagram of beam profile*

To delineate a narrower pattern with a certain beam profile, the exposure dose would have to be decreased to locate the threshold level at the upper part of the beam profile, which has a smaller width. However, the LER becomes larger owing to the smaller slope at the upper part of the beam profile, and the pattern is unresolved (see Fig. 4).

The actual mechanism that determines the RL in EB lithography has been identified experimentally, which demonstrates that the RL depends on beam blur. A smaller beam blur causes a steeper slope, which results in a smaller LER and a higher RL.

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M. Yoshizawa and S. Moriya (*ULSI R&D Laboratories, Sony Corporation, 4-14-1, Asahi-cho, Atsugi-shi, Kanagawa-Ken, 243-0014, Japan*)

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Ti/Pt/Au ohmic contacts on *p*-type GaN/$Al_xGa_{1-x}N$ superlattices

L. Zhou, A.T. Ping, F. Khan, A. Osinsky and I. Adesida

The electrical characteristics of Ti/Pt/Au contacts on *p*-type GaN/$Al_xGa_{1-x}N$ (x = 0.10 and 0.20) superlattices (SL) have been investigated. Current-voltage and specific contact resistance measurements indicate enhanced *p*-type doping in the superlattice structures compared to that in GaN. Ti/Pt/Au is demonstrated to be an effective ohmic metallisation scheme for GaN/$Al_xGa_{1-x}N$ superlattices. A low specific contact resistance of 4.6×10^{-4} Ωcm² is reported for unalloyed Ti/Pt/Au on an GaN/$Al_{0.2}Ga_{0.8}N$ SL.

Low resistance ohmic contacts are essential for improving the electrical and optical performance of devices based on GaN-based materials. For *n*-type GaN, metallisation schemes in which Ti is used have been very successful in lowering the specific contact resistance (R_c) to less than $10^{-5}\Omega cm^2$ [1 – 3]. On the other hand, owing to the wide bandgap and the relatively deep acceptor level of the commonly used Mg dopant, there has been great difficulty in finding ohmic contacts with $R_c < 10^3\ \Omega cm^2$ for *p*-GaN [4]. To date, there are only three ohmic metallisation and processing schemes for *p*-GaN that have yielded $R_c < 10^{-3}\Omega cm^2$. In one of these methods a post-metallisation anneal of 10min at 800°C is required [5], while in another a boiling aqua regia surface treatment is required prior to metal deposition [6, 7]. The third method involves deliberate oxidation of the metallisation at 500°C for 10min [8]. To make the metallisation process more compatible with device processing, it is desirable to find a low-resistance ohmic contact for *p*-GaN which requires less aggressive chemical treatments and relaxed annealing conditions.

As originally proposed by Schubert *et al.* [9], the overall hole concentration in a *p*-type semiconductor can be increased through the generation of valence band edge oscillations in a superlattice. This technique improves the activation efficiency of deep acceptors by allowing them to ionise when tunnelling occurs from the larger bandgap material into the adjacent material with a narrower bandgap. Indeed, significantly enhanced *p*-type doping efficiency in GaN/$Al_xGa_{1-x}N$ short-period superlattices (SLs) has been reported recently [10, 11]. In this Letter, we demonstrate excellent ohmic contacts on GaN/$Al_xGa_{1-x}N$ SL with a Ti/Pt/Au metallisation scheme which does not require any aggressive surface treatment and post-metallisation anneal. The results are compared to those obtained from the same metallisation on *p*-GaN.

The superlattice layers used in this study were grown by MBE on sapphire and consisted of 20 periods each of Mg-doped GaN (10nm) and $Al_xGa_{1-x}N$ (10nm). Samples with two different aluminium concentrations, x = 0.1 and 0.2, were investigated. Both

samples exhibited a mobility of ~1cm^{2}V^{-1}s^{-1} from room temperature Hall measurements. The reference p-GaN layer used in this study had a 0.3μm doped layer with a nominal bulk carrier concentration of 2.5×10^{17}cm^{-3} and a mobility of 9cm^{2}V^{-1}s^{-1} as obtained from Hall measurements at room temperature. Contact resistances were determined using the linear transfer length method (TLM). The structures used for the TLM measurements were fabricated by first patterning the p-GaN and SL samples with $100 \times 650\mu m^2$ mesas. The pattern was then transferred into the samples using reactive ion etching, which electrically isolated the mesas. Rectangular pads were then patterned. Prior to transferring the samples into the evaporation chamber, the surfaces were cleaned in O_2 plasma, followed by dips in a dilute HCl:DI (1:2) solution. Electron beam evaporation was used to deposit Ti (15nm) and Pt (50nm), while Au (80nm) was thermally evaporated as the last capping layer. The contact characteristics were studied using current-voltage (I-V) and four-probe linear TLM techniques at room temperature. For accurate specific contact resistance determination, actual pad spacings were determined using scanning electron microscopy (SEM) after metal lift-off.

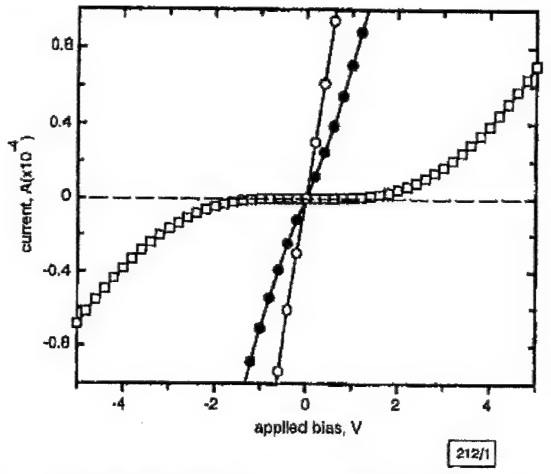

Fig. 1 *Current-voltage characteristics of as-deposited Ti/Pt/Au contacts on p-type GaN and GaN/Al$_x$Ga$_{1-x}$N superlattices (x = 0.1 and 0.2)*

□ p-GaN
● $Al_{0.1}Ga_{0.9}N$/GaN-SL
○ $Al_{0.2}Ga_{0.8}N$/GaN-SL

Fig. 1 shows the current-voltage characteristics of as-deposited Ti/Pt/Au contacts on all three samples. The as-deposited contact is rectifying on the reference p-type GaN. In contrast, owing to the enhanced doping efficiencies, the I-V curves for GaN/Al$_x$Ga$_{1-x}$N SL exhibit better linearity. Fig. 1 also reveals that the sample with a higher aluminium mole fraction (x = 0.2) was more ohmic in its I-V characteristics. This is consistent with a calculated carrier concentration of 3×10^{18}cm^{-3} for the SL (x = 0.1) compared with 5×10^{18}cm^{-3} for the other (x = 0.2). An additional mechanism in support of this observation is that the total polarisation charge should be higher in the SL with x = 0.2 [10].

Table 1: Summary of results of as-deposited Ti/Pt/Au contacts on p-type GaN and GaN/Al$_x$Ga$_{1-x}$N superlattices (x = 0.1 and 0.2)

Semiconductor layer structure	Contact resistivity	Specific contact resistance
	Ωmm	Ωcm^2
p-GaN	Schottky	Schottky
GaN/$Al_{0.1}Ga_{0.9}N$ SL	71.9	6.6×10^{-4}
GaN/$Al_{0.1}Ga_{0.9}N$ SL	40.7	4.6×10^{-4}

The contact resistivity (ρ_c) and specific contact resistance (R_c) were calculated from the measured resistance against contact pad spacing data using the linear TLM method. Fig. 2 shows the data of the measured resistance against pad distance for the as-deposited Ti/Pt/Au contacts on the two SL samples. Least-squares linear regression lines were used to extrapolate the data to the y-axis. The slope of the regression line is a measure of the sheet resistance of the semiconductor. It is clear that the SL with x = 0.2 has a smaller slope and therefore a lower sheet resistance, again due to the increased carrier concentration owing to its higher Al mole fraction. ρ_c and R_c values can be extracted from the slope of the line, x- and y-intercepts and the pad width. These results are summarised in Table 1. For contacts on semiconductors with $N_A > 10^{17}$cm^{-3}, the tunnelling process will dominate. In this case, $R_c \propto \exp[m(N_A)^{-1/2}]$, where m is a parameter related to the contact barrier height and hole effective mass, and N_A, which is the effective carrier concentration. It is clear from this relationship that R_c will be lower for the SL with x = 0.2, and the R_c of both SL should be much lower than that of the p-GaN, which is consistent with the results shown in Fig. 1 and Table 1.

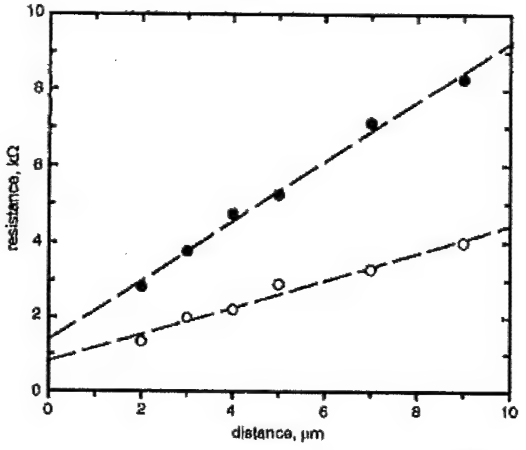

Fig. 2 *Measured resistance against contact spacing for as-deposited Ti/Pt/Au contacts on p-type GaN/Al$_x$Ga$_{1-x}$N superlattices (x = 0.1 and 0.2)*

· · least-squares linear regression lines fitted to different data sets
● $Al_{0.1}Ga_{0.9}N$/GaN-SL
○ $Al_{0.2}Ga_{0.8}N$/GaN-SL

There are a number of reasons for adopting Ti/Pt/Au metallisation for this study. According to the Schottky-Mott model of metal-semiconductor contacts, the metal-semiconductor barrier height ϕ_b is related to the work function of the metal ϕ_m and the electron affinity of a p-type semiconductor χ_s by $\phi_b = (\chi_s + E_g) - \phi_m$, if there is no Fermi level pinning at the M-S interface. Therefore to reduce the barrier height, choosing metals with high work functions is almost inevitable. Pt, with a ϕ_m of 5.65eV, has the highest work function of all metals and is chemically stable. However, experiments have shown that Pt alone suffers from poor adhesion on GaN and, therefore, a thin Ti layer is used to improve adhesion as well as getter surface contamination or oxides. The excellent ohmic contacts obtained here for Ti/Pt/Au shows that Ti has been effective in these roles. Investigations are now being initiated to determine the effectiveness and stability of Ti/Pt/Au contacts on p-type GaN and Al$_x$Ga$_{1-x}$N alloys after heat treatments.

In conclusion, we have presented the electrical characteristics of Ti/Pt/Au contacts on p-type GaN/Al$_x$Ga$_{1-x}$N superlattices. The results indicate that an effective increase in carrier concentration can be obtained by using superlattice structures. The Ti/Pt/Au scheme has been demonstrated to be an effective ohmic metallisation scheme for GaN/Al$_x$Ga$_{1-x}$N superlattices, in which a specific contact resistance of 4.6×10^{-4} Ωcm^2 has been obtained for a GaN/$Al_{0.2}Ga_{0.8}N$ superlattice without any heat treatment.

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L. Zhou, A.T. Ping, F. Khan and I. Adesida (*Microelectronics Laboratory, Department of Electrical and Computer Engineering, University of Illinois, Urbana-Champaign, IL 61801, USA*)

A. Osinsky (*NZ Applied Technologies, Woburn, MA 01801, USA*)

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Ultrafast coherent all-optical switching in quantum-well semiconductor microcavity

C. De Matos, M. Pugnet and A. Le Corre

Picosecond degenerate four-wave mixing experiments at room temperature in a GaInAs-GaInAsP multiple quantum well embedded in a microcavity are presented. An input diffraction efficiency of 2% with only 1μJ/cm² pump fluence is achieved. The authors show that the diffraction phenomenon is ultrafast and coherent. For a photon energy 30meV below the exciton band edge and for low pump intensities (1μJ/cm²), the diffraction phenomenon is not perturbed by strong and spatially uniform pump pulse pre-illumination. This result demonstrates the potential of semiconductor microcavities for the realisation of ultrafast, sensitive and coherent devices.

Introduction: Nonlinear semiconductor materials coupled to Fabry-Perot (FP) microcavities are promising devices for the implementation of ultrafast and sensitive two-dimensional optical information processing systems such as optical spatial reconfigurable interconnections and coherent optical gate or optical time demultiplexing. Future telecommunication networks will require devices with a response time in the subpicosecond range. A common means of obtaining fast semiconductor components is to modulate the dielectric function by exploiting the presence of free photogenerated carriers which have a short lifetime [1, 2]. However, these structures require a relatively high free-carrier density and so the high-bit-rate processing is limited by thermal problems [3]. One way of avoiding such problems would be to use non-dissipative physical effects, which although weak can be enhanced using microcavities [4, 5]. Recently, degenerate four-wave mixing (DFWM) experiments on a multiple quantum-well (MQW) structure enclosed in an FP microcavity have demonstrated that coherent effects at room temperature via virtual third-order nonlinearities can induce diffraction phenomena [5].

Sample and experiment: The MQW sample was grown by gas source molecular beam epitaxy on an *n*-type InP substrate. The MQW consisted of 50 periods of 6.7nm GaInAs wells and 8nm GaInAsP barriers, presenting an excitonic absorption peak at a wavelength of 1.56μm. To process the cavity, we decided against using semiconductor Bragg reflectors because the index difference between the available materials in the InP family is too weak. To process the cavity, we opted instead for the epitaxial lift-off technique. The epitaxial layers were bonded on a gold layer to realise a back mirror ($R \simeq 100\%$) and a dielectric Bragg reflector composed of four stacks of e-beam TiO_2/SiO_2 layers was deposited on top of the structure, to realise the front mirror with a reflectivity adjusted to 80% around 1.55μm [6].

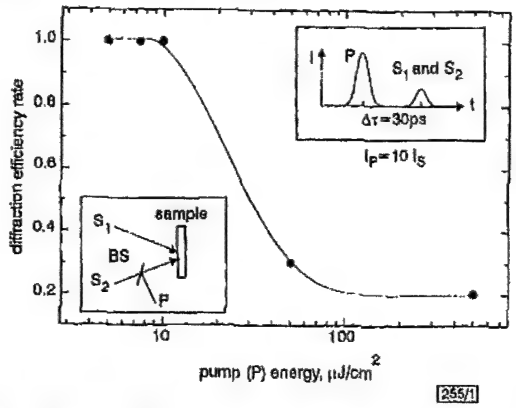

Fig. 1 *Diffraction efficiency rate against pump (P) energy density*

For low pump energies, diffraction phenomenon was not affected by pump pulse pre-illumination
- - - guide to eyes
BS: beam splitter

DFWM experiments using an optical parametric oscillator with a pulse duration of 15ps were performed on the sample described above. The laser beam was first split into two pulses (P and S), with respective intensities of $I_P = 10I_S$. Beam S was then split again into two new beams (S_1 and S_2), with nearly equal intensities, and focused on the sample with a 40cm focal length lens. The wave vectors of the two S beams were, respectively, $\mathbf{k}_1$ and $\mathbf{k}_2$ and formed an angle of 0.05 rad. The diffracted signal was detected in the direction $\mathbf{k}_d = 2\mathbf{k}_1 - \mathbf{k}_2$ with a slow Ge detector. The pump beam (P) was focused in the same manner as the S beams and in the same direction as S_2 ($\mathbf{k}_2$) but arrived at the sample 30ps before the S pulses. We were thus able to study the behaviour of the device when a spatial uniform pump pulse arrived before the switching operation and could therefore simulate ultrahigh-bit-rate processing, for example the influence of the photogenerated free carriers on the diffraction phenomena. The wavelength of the three beams was maintained during the experiment at 1.62μm, corresponding to an incident photon energy 30meV below the excitonic bandgap.

Results and discussion: The DFWM signal obtained with and without pump pulse (*P*) for different fluences is shown in Fig. 1. The pump pulse arrives 30ps before the S pulses. The diffraction efficiency rate shown in Fig. 1 is defined as the ratio of the diffracted signal with the pump pulse to the diffracted signal without the pump pulse. For a pump fluence of 500μJ/cm², the diffraction efficiency is reduced strongly and only 20% is maintained. This effect can be easily understood in terms of free-carrier occupation regime (FCO). Indeed, at these fluences, the diffraction phenomenon occurs due to the spatial modulation of the dielectric function via the spatial modulation of the free-carrier density. In this case,

Plasma-induced damage study for *n*-GaN using inductively coupled plasma reactive ion etching*

F. A. Khan, L. Zhou, V. Kumar, and I. Adesida[a)]
Department of Electrical and Computer Engineering and Microelectronics Laboratory, University of Illinois, Urbana, Illinois 61801

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In this article, we report a comprehensive study on plasma-induced damage for *n*-GaN using inductively coupled plasma (ICP) reactive ion etching. Effect of ICP coil power, etch duration and bias voltage on the electrical characteristics of *n*-GaN was investigated. It was observed that variation in ICP coil power and etch duration had minimal effect on varying the plasma-induced surface damage. Bias voltage was found to be the most significant cause of variation in plasma-induced damage to the surface of *n*-GaN. Therefore, low surface damage can be achieved by optimizing the bias voltage at which the sample is being etched. Auger electron spectroscopy analysis showed that the stoichiometry of the etched GaN surfaces was identical, independent of the etching conditions. © *2001 American Vacuum Society.* [DOI: 10.1116/1.1418415]

I. INTRODUCTION

GaN is an excellent material for fabricating novel devices which are capable of operating under extreme conditions. Some examples of GaN-based devices include, heterojunction bipolar transistors, high electron mobility transistors and thyristors for high temperature and high power applications. Due to GaN's inert chemical nature and high bond energies, it is resistant to most wet chemical etchants, making device patterning mostly dependent on dry etching. A number of dry etching techniques and plasma chemistries have been reported for etching a wide range of GaN-based materials.[1–14] Etch chemistries have been largely based on Cl_2 mixtures while techniques used include chemically assisted ion beam etching,[1–3] reactive ion etching (RIE),[4–7] electron-cyclotron-resonance reactive ion etching,[8–10] magnetron reactive ion etching[11] and inductively coupled plasma reactive ion etching (ICP-RIE).[12–14] However, to date, there has been a paucity of work on the systematic characterization of ICP-RIE plasma-induced damage on GaN surfaces. Some of the most recent studies have claimed that even short ICP-RIE plasma exposures ($\leqslant$ 4 s) can have drastic effects on the electrical characteristics of the surface of *n*-GaN.[15–17] Therefore, it is essential to find plasma conditions that produce low surface damage in order to tailor etching processes for optoelectronic and power electronic devices based on GaN.

In this article, we present our work on systematically studying ICP-RIE plasma-induced damage on the surface of *n*-GaN using Cl_2/Ar gas chemistry. Effects of ICP coil power, etch duration and bias voltage on the barrier height, ϕ_b, ideality constant, n, reverse breakdown voltage, V_b, and forward turn on voltage, V_f, were extensively investigated.

II. EXPERIMENT

A Plasma-Therm Shuttlelock 700 ICP-RIE system was used to study the effects of plasma-induced damage on the surface of *n*-GaN. A plasma enhanced chemical vapor deposition oxide mask was used for the etch rate study. The oxide mask was removed in buffered oxide etch before the etched depth was measured using a profilometer. For the plasma-induced damage study, ohmic contacts to the *n*-GaN were first formed by rapid thermal annealing of evaporated Ti/Al/Ti/Au at 850 °C for 60 s. The samples were then etched in the ICP-RIE using Cl_2/Ar gas chemistry. The etched samples were rinsed in 1:1 HCl:H_2O solution before evaporating Ni/Au Schottky contacts on them. The Cl_2/Ar flow rate and chamber pressure were kept constant at 14/6 sccm and 3 mT, respectively for all plasma exposures. ICP coil power and bias voltage were varied between 100 and 500 W and −50 to −200 V, respectively. The ICP coil power controls the dissociation of the plasma and the incident ion flux while the bias voltage controls the incident ion energy. Diode characteristics were measured on a HP4142B parameter analyzer. Reverse breakdown voltage, V_b, was defined as the reverse voltage at which the leakage current was 10^{-3} A. Forward turn-on voltage, V_f, was defined as the voltage where the tangent to the $I-V$ curve intersected with the voltage axis. $C-V$ measurements were also performed using a HP4280A impedance analyzer on the Schottky diodes to determine the barrier height and the epitaxial doping concentration. The trends in variation of barrier height obtained using $I-V$ measurements were identical to those obtained using $C-V$ measurements. Moreover, $C-V$ measurements also indicated that Cl_2/Ar etching conditions being investigated had very little effect on the charge density of the etched *n*-GaN samples.

III. RESULTS AND DISCUSSION

Figure 1 shows the etch rate of *n*-GaN as a function of ICP coil power for different bias voltages. The etch rate was found to be dependent on both the ICP coil power and the bias voltage. ICP coil power controls the density of the ionized gaseous species in the chamber while the bias voltage controls the energy with which the ions strike the substrate. The etch rate is dependent on both the surface chemical reactions to produce volatile species and physical sputtering

*No proof corrections received from author prior to publication.

a)Electronic mail: iadesida@uiuc.edu

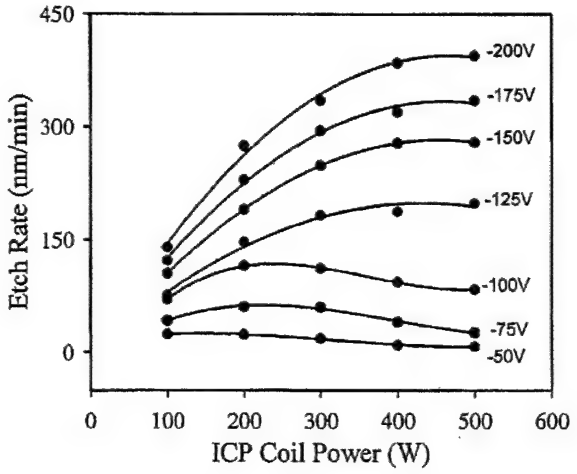

FIG. 1. Etch rate vs ICP coil power for different dc bias voltages. (Pressure=3 mT; gas flow rate=14/6 sccm of Cl_2/Ar.)

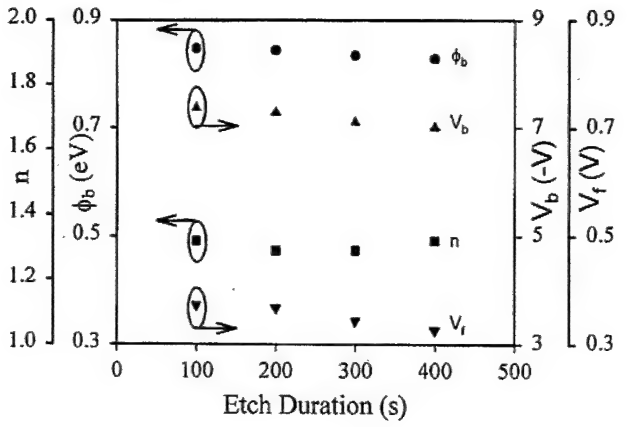

FIG. 3. Au/Ni/*n*-GaN Schottky diodes ϕ_b, n, V_b, and V_f as a function of etch duration. (ICP coil power=300 W; bias voltage=−100 V, pressure=3 mT; gas flow rate=14/6 sccm of Cl_2/Ar.)

mechanisms responsible for removing the volatile species from the surface. A downward shift in the etch rate curves can be attributed to either the surface chemical reactions or physical sputtering mechanisms to be the limiting step.

Figure 2 shows the variation in ϕ_b, n, V_b, and V_f as a function of ICP coil power. The bias voltage was kept constant at −100 V. All samples were etched for a duration of 120 s. The values for ϕ_b, n, V_b, and V_f for the control sample were 848 meV, 1.6, −7.45 V and 470 mV, respectively. Increasing the ICP coil power from 100 to 500 W produced very little variation in the values for ϕ_b, n, V_b, and V_f in the etched samples.

Figure 3 shows the variation in ϕ_b, n, V_b and V_f as a function of etch duration. The ICP coil power and bias voltage were kept constant at 300 W, −100 V, respectively. The values for ϕ_b, n, V_b, and V_f for the control sample were 905 meV, 1.61, −8.78 V and 480 mV, respectively. As the etch duration was increased from 100 to 400 s, the values for ϕ_b, V_b, and V_f decreased from 850 to 830 meV, −7.4 to −7.0 V and 372 to 326 mV, respectively. Therefore, it can be concluded that if we take into account experimental error, variation in the etch duration for the experimental conditions being studied produced very little variation in the values of ϕ_b, n, V_b, and V_f in the etched samples. Therefore, bias voltage rather than plasma exposure duration is the significant cause of plasma-induced damage.

Figure 4 shows the room temperature $I-V$ characteristics of Schottky diodes formed on *n*-GaN samples etched at different bias voltages. The ICP coil power was kept constant at 300 W. As expected, increasing the bias voltage increased the plasma-induced damage on the etched *n*-GaN surfaces. As pointed out above, increasing the bias voltage increases the energy with which the ions bombard the surface of the substrate. Therefore increasing the bias voltage would tend to increase the plasma-induced damage. V_b for the control sample was −5.85 V.

Figure 5 plots the variation in ϕ_b, n, V_b and V_f as a function of bias voltage. The ICP coil power was kept constant at 300 W. All samples were etched to, approximately, a

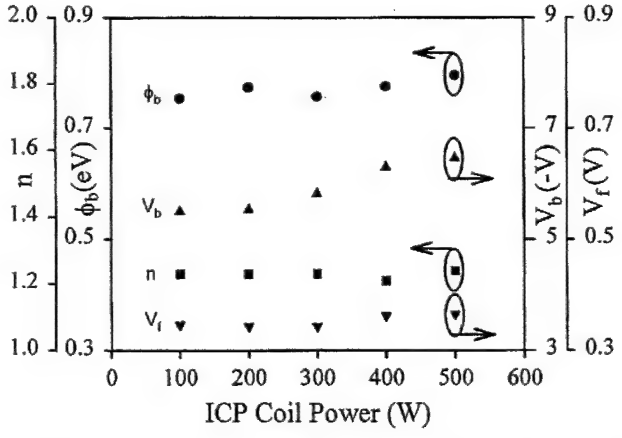

FIG. 2. Au/Ni/*n*-GaN Schottky diodes ϕ_b, n, V_b, and V_f as a function of ICP coil power. (Bias voltage=−100 V; pressure=3 mT; gas flow rate=14/6 sccm of Cl_2/Ar; etch duration=120 s.)

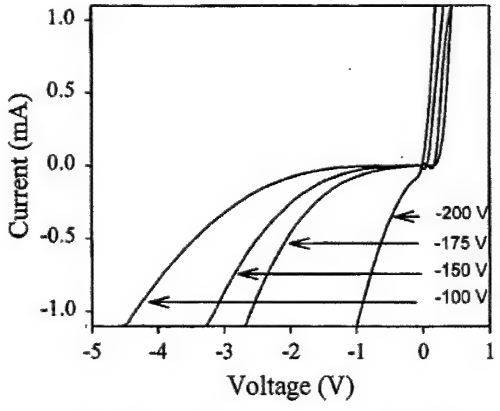

FIG. 4. Room temperature $I-V$ characteristics of Ni Schottky barrier diodes formed directly on the etched *n*-GaN surfaces for constant time at different bias voltages. (ICP coil power=300 W; pressure=3 mT; gas flow rate=14/6 sccm of Cl_2/Ar; etch duration=100 s.)

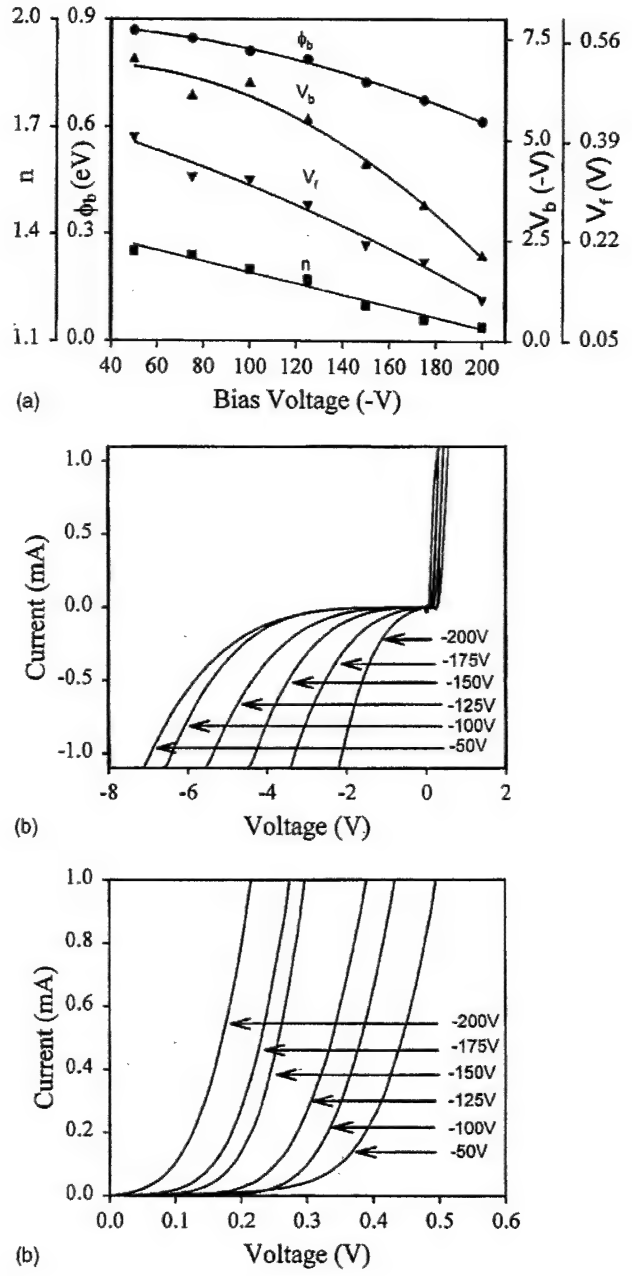

FIG. 5. (a) Au/Ni/*n*-GaN Schottky diodes ϕ_b, n, V_b, and V_f as a function of bias voltage for *n*-GaN samples etched to a constant depth at different bias voltages; (b) room temperature $I-V$ characteristics; (c) room temperature forward $I-V$ characteristics. (ICP coil power=300 W; pressure=3 mT; gas flow rate=14/6 sccm of Cl_2/Ar; etch depth=2500 Å.)

constant depth of 2500 Å. Owing to the different etch rates corresponding to different bias voltages, the samples were exposed to the plasma for different duration to etch a constant depth of 2500 Å. It is interesting to observe that in spite of the difference in plasma exposure duration, the plasma-induced damage increased with the bias voltage. The sample etched at −50 V was exposed to the plasma for 835 s while that etched at −200 V was exposed to the plasma for only 45 s to achieve a constant etched depth of 250 nm. Despite this

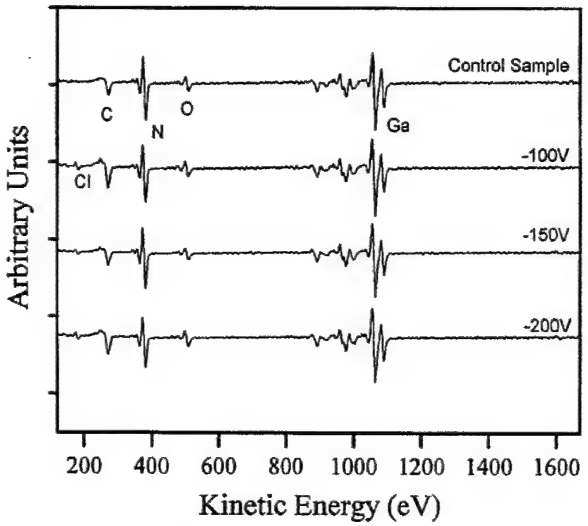

FIG. 6. AES of unetched *n*-GaN and *n*-GaN etched at −100, −150, and −200 V. (ICP coil power=300 W; pressure=3 mT; total gas flow rate=14/6 sccm of Cl_2/Ar; etch duration=100 s.)

substantial difference in the plasma exposure duration, the electrical characteristics of the sample etched at −50 V were significantly better than those of sample etched at −200 V. This confirms our earlier observations that the bias voltage rather than the plasma exposure duration is the more significant cause of the plasma-induced damage. As the bias voltage was increased from −50 V to −200 V, ϕ_b, V_b, and V_f decreased from 869 to 615 meV, −7 to −2.1 V, and 400 to 121 mV, respectively. The terms ϕ_b, V_b, and V_f for the control sample were 883 meV, −7.20 V, and 434 mV, respectively. Figure 5(b) shows how the reverse breakdown voltage was affected by the variation in bias voltage from −50 to −200 V. Figure 5(c) shows how the forward turn-on $I-V$ characteristics of the etched samples changed as the bias voltage was increased from −50 to −200 V.

Auger electron spectroscopy (AES) analysis was performed on etched GaN layers to investigate etch-induced surface stoichiometric changes. Figure 6 shows the AES spectra of an unetched control sample in comparison with those etched at −100, −150, and −200 V. ICP coil power, chamber pressure, gas flow rate, and etch duration was kept constant at 300 W, 3 mT, 14/6 sccm of Cl_2/Ar and 100 s, respectively. The surfaces of all samples were cleaned in 1:1 HCl:H_2O solution before being analyzed. The C and O peaks in the various spectra are due to the atmospheric exposure. The Cl in the spectra of the etched sample is from the etchant gas.[18] Within experimental error, the relative concentration of N, and Ga on the etched samples was observed to be identical to the unetched control sample.

IV. CONCLUSIONS

In summary, plasma-induced damage caused by inductively coupled plasma reactive ion etching in Cl_2/Ar gas mixtures on GaN was extensively investigated. ICP coil power and plasma exposure duration were found to affect the

plasma-induced damage minimally. Bias voltage was found to be the most significant cause of the plasma-induced damage. Auger electron spectroscopy of the etched samples showed that the plasma etching conditions being investigated produced very little variation in the surface stoichiometry of the etched samples.

ACKNOWLEDGMENT

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Thermal stability of rhenium Schottky contacts on *n*-type $Al_xGa_{1-x}N$

L. Zhou,[a] F. A. Khan, G. Cueva, V. Kumar, and I. Adesida
Department of Electrical and Computer Engineering and Microelectronics Laboratory, University of Illinois, Urbana, Illinois 61801

M. R. Sardela, Jr.
Materials Research Laboratory, University of Illinois, Urbana, Illinois 61801

F. D. Auret
Department of Physics, University of Pretoria, Pretoria 0002, South Africa

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The impact of rapid thermal annealing on the electrical and materials characteristics of Re Schottky contacts on *n*-type GaN and $Al_xGa_{1-x}N$ ($x=0.10$ and 0.26) was investigated. Effective barrier heights were obtained from current–voltage and modified Norde measurements on diodes annealed at up to 800 °C. For $Al_xGa_{1-x}N$ with $x>0$, Schottky barrier heights were found to increase upon annealing from the as-deposited state, but decreased sharply after annealing at 600 °C. Modified Norde measurements indicate that this degradation could be explained by the existence of a shunt conduction path with an associated barrier height below 0.46 V, possibly a consequence of an inhomogeneous interface after annealing at temperatures above 600 °C. A new defect lying at 0.34 eV below the conduction band edge was also detected by deep level transient spectroscopy after contact degradation. © *2002 American Institute of Physics.* [DOI: 10.1063/1.1503402]

Thermally stable Schottky contacts are essential for the realization of self-aligned high electron mobility field-effect transistors (HEMTs) in the GaN/AlGaN materials system. Successful fabrication of such a device requires the Schottky gate to withstand a source/drain contact annealing process without significant barrier degradation. Typical Ti/Al-based source/drain ohmic contacts for GaN/AlGaN HEMTs require annealing between 750 °C–850 °C for 30 s to achieve minimum resistance. In addition, $x>0.20$ is required for the $Al_xGa_{1-x}N$ layer to maximize the two-dimensional electron gas charge density in the HEMT channel. Of the few systematic annealing studies on metal/$Al_xGa_{1-x}N$ Schottky contact systems,[1,2] none approaches the materials-temperature performance envelope defined by the HEMT requirements stated herein. Rhenium Schottky contacts were recently studied for their stability on GaN, GaAs, and 6H–SiC,[3–5] and it was predicted, based on thermodynamic arguments, to be one of the more promising candidates for stable contacts on $Al_xGa_{1-x}N$.[6] This letter reports the Schottky barrier characteristics of Re/$Al_xGa_{1-x}N$ contact system ($x=0$, 0.10, and 0.26) after annealing at temperatures between 300 °C–800 °C.

The $Al_xGa_{1-x}N$ layers used for this study consisted of 3 μm thick undoped $Al_xGa_{1-x}N$ followed by 1 μm of Si-doped $Al_xGa_{1-x}N$. Bulk carrier concentrations of the doped layers were determined by capacitance–voltage measurements to be about 2.5×10^{17} cm^{-3}. The reference GaN layer used in this study had a similar structure with a nominal bulk carrier concentration of 1.4×10^{17} cm^{-3}. The measured device structure consisted of an array of 250 μm diameter Schottky dots separated 25 μm radially from the Ti/Al-based ohmic contact. Prior to transferring the samples into the metal evaporation chamber, $Al_xGa_{1-x}N$ surfaces were cleaned with an O_2 plasma asher, followed by dips in dilute HF:DI solutions. Electron-beam evaporation was used to deposit Re (99.9% pure, supplied by Pure Tech, NY) to a thickness of 80 nm. After the lift-off process, different diodes were annealed in a rapid thermal annealing furnace in a 1 atm N_2 ambient for 1 min between 300 °C and 800 °C in 100 °C intervals. Schottky diode characteristics were measured using current–voltage ($I-V$) and modified Norde ($I-V-T$) techniques.

Flatband barrier heights (ϕ_{bf}) plotted in Fig. 1 were calculated from

$$\phi_{bf}=n\phi_{b0}-(n-1)(kT/q)\ln(N_c/N_d), \tag{1}$$

where the zero-bias barrier height, ϕ_{b0}, and ideality, n, were determined using forward-bias $\log I$ versus V characteristics of Re contacts on $Al_xGa_{1-x}N$. N_c is the effective density of states for the conduction band, N_d is the ionized dopant concentration, and other symbols carry their usual meanings. $Al_xGa_{1-x}N$ materials parameters used in calculating ϕ_{b0}

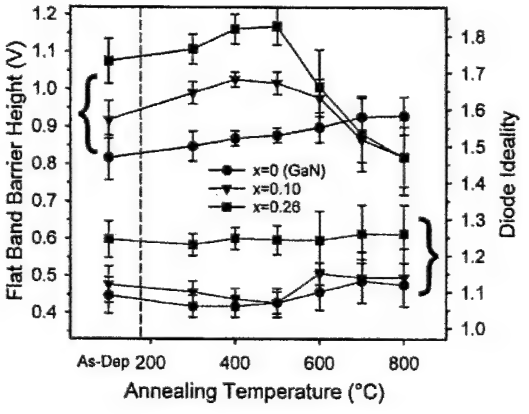

FIG. 1. Flatband barrier height and diode ideality factor of rhenium contacts on $Al_xGa_{1-x}N$ ($x=0$, 0.1, and 0.26) before and after heat treatments.

[a]Electronic mail: lingzhou@uiuc.edu

were given elsewhere.[7] Regardless of the aluminum concentration, Re diodes on AlGaN all improved significantly upon annealing, reaching a peak barrier height after annealing at around 400 °C–500 °C as shown in Fig. 1. More intimate metal–semiconductor contacts after annealing resulted in idealities reducing slightly toward 1, indicating a better fit to the thermionic emission model. At these moderate annealing temperatures, the uniformity of the fabricated diodes also improved markedly as seen by the reduction of data scatter in both diode ideality and barrier height. The behavior of Re on GaN is consistent with an earlier report.[3] In contrast to Re/GaN, Re/AlGaN diodes exhibited significant reductions in barrier heights after annealing at 600 °C and above. Uniformity also suffered after annealing at higher temperatures. In conjunction with the reduction in barrier heights, reverse leakage current densities were also observed to increase by about 5 orders of magnitude after an 800 °C anneal from their 400 °C values: From 2×10^{-9} to 1.8×10^{-4} A cm^{-2} at -10 V for Re/$Al_{0.1}Ga_{0.9}N$, for example.

To avoid potential errors due to high series resistances on the extracted ϕ_b at high Al concentrations and avoid making assumptions on the Richardson constant of the diodes, Schottky barrier heights were also extracted with the $I-V-T$ method, following procedures given by Tam *et al.*[8] and Schmitz *et al.*[9] $I-V-T$ measurements were conducted by placing samples on a variable temperature probe station housed inside a nitrogen-purged environmental chamber. Forward $I-V$ curves were collected at 15 °C intervals from -55 °C to 95 °C. To reduce clutter in Fig. 2(a), typical forward I versus V plots of Re/$Al_{0.26}Ga_{0.74}N$ were given at only three of the eleven measurement temperatures: -55 °C, 20 °C, and 95 °C, after annealing the diodes at 400 °C, 600 °C, and 800 °C. In addition to the increased forward current due to lower barrier heights, the most significant change after high-temperature annealing is the increased low-bias current, readily apparent by comparing the sets of log $I-V$ curves obtained at -55 °C and 20 °C but annealed at three different temperatures. Figure 2(b) shows the $2F1_m+(2-n)\ln(I_m/T^2)$ versus q/kT plot used to extract the barrier heights from $I-V-T$ measurements. $F1_m$ is the minimum of the function $F1=(qV/2kT)-\ln(I/T^2)$ and the corresponding minimum in diode current I measured at any given temperature.[9] The slope of each line is directly proportional to the barrier height of the diode, which in this case is closer to the zero-bias barrier height (ϕ_{b0}) than flatband barrier height (ϕ_{bf}) obtained from $I-V$ measurements. Figure 2(b) revealed a second, lower barrier for diodes annealed at 800 °C. Without knowing the ideality of this lower barrier, the slope gives its upper limit as 0.46 V. For Re/$Al_xGa_{1-x}N$ diodes with $x=0$, 0.1, and 0.26, the Richardson constants were on the order of 20, 1.0, and 0.1 A cm^{-2} K^{-2}, respectively, after moderate annealing and before barrier degradation. Vertical separation of the two segments in Fig. 2(b) after high-temperature annealing indicates different Richardson constants associated with each barrier. Because this barrier only appears at lower measurement temperatures (higher q/kT values), it is very likely due to the formation of inhomogeneous diodes with low-barrier "patches" at the Re–AlGaN interface as a result of interfacial reactions. Since current I is proportional to $\exp(-\phi_b/kT)$, at a small bias and low T, a contribution to the forward current may predominantly come from the portion of an inhomogeneous diode with the least barrier height, even when the low-barrier region only occupies a small fraction of the interface. This explains the segmented appearance of the lines with different slopes in Fig. 2(b), and the fact that the low-barrier height segments show up only at low temperatures when their contribution to the overall current is dominant. For diodes fabricated on $Al_{0.1}Ga_{0.9}N$, segmentation also happens after high-temperature annealing but the second-barrier height is not as well defined.

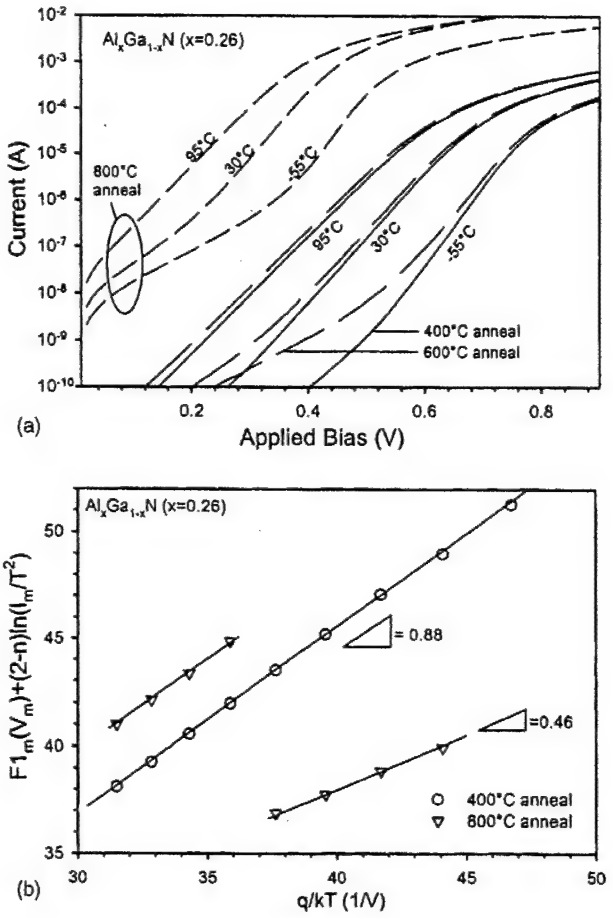

FIG. 2. (a) Selected $I-V-T$ results of annealed diodes. Forward log I vs V curves were shown for only three of the eleven measurement temperatures after annealing. (b) Barrier heights extracted from $I-V-T$ measurements, showing a low-barrier segment after annealing at 800 °C.

Low-bias anomalies in Schottky diodes, similar to those shown in Fig. 2(a), in which the diode current is higher than expected from thermionic emission alone, are often attributed to a variety of factors other than diode inhomogeneity, such as recombination–generation (R–G) currents and edge effects. However, close examination points to interface inhomogeneity as the most likely origin.[10] In addition, it was reported that when the low-bias anomaly was believed to be due to R–G centers, the reverse leakage current does not increase substantially,[11] which is contrary to what we have observed in the Re/AlGaN system, where we saw a 10^5 increase in reverse leakage current after high-temperature annealing.

A deep level transient spectroscopy (DLTS) study was

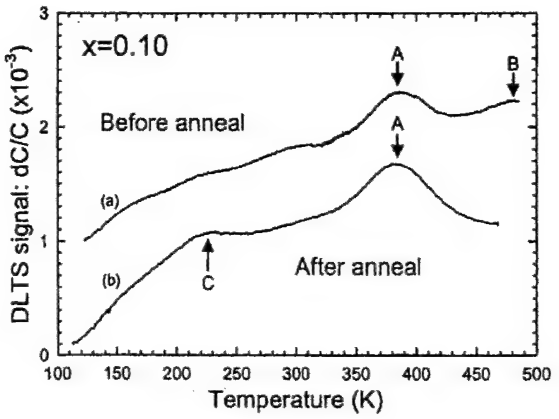

FIG. 3. DLTS spectra of Re on $Al_{0.1}Ga_{0.9}N$ obtained before (a) and after (b) annealing at 800 °C for 1 min.

carried out to examine the formation of new defect centers that might be responsible for the low-bias $I-V$ anomaly. Since diodes fabricated on $Al_{0.1}Ga_{0.9}N$ exhibited much better uniformity and excellent ideality compared to those fabricated on $Al_{0.26}Ga_{0.74}N$, DLTS study was carried out on these diodes so that potential defects could be more easily isolated. Figure 3 shows that defect B was annealed out while a new trap C appeared after rapid thermal annealing. Defect B has a bandlike energy distribution, located at about 0.7–0.9 eV below the conduction band edge, and may be attributed to electron-beam (e-beam) damage. It was previously shown that e-beam deposition introduces defects in n-GaN and that these defects lead to inferior device performance.[12] Defect C is located at about 0.34 eV below band edge with an apparent capture cross section $\sigma=1\times10^{-16}$ cm^{-2}. Defect A which persisted after annealing has an activation energy of 0.77 eV with $\sigma=8\times10^{-15}$ cm^{-2}, and its population did not change upon annealing.

Further examinations of the annealed Re/AlGaN system by x-ray diffraction (XRD) were shown in Fig. 4. To increase the likelihood of detecting intermetallic reaction products, another AlGaN wafer with relatively high Al concentration ($x=0.22$) was used, and the Re/$Al_{0.22}Ga_{0.78}N$ samples were annealed at 400 °C and 800 °C for 30 min rather than 1 min.

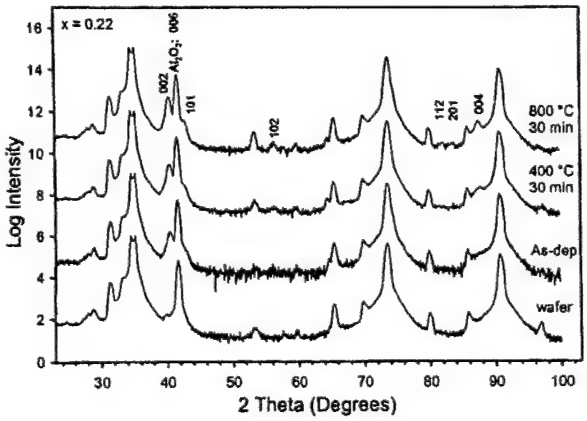

FIG. 4. XRD scans of the Re/$Al_{0.22}Ga_{0.78}N$ contact system before and after heat treatments. The annealing time was 30 min at each marked temperature. Al_2O_3(006) was used for scan calibration, other indexed peaks belong to rhenium.

Since barrier degradation occurred near the melting point of Al, special attention was paid to possible eutectic alloys between Re–Al, which are known to form at moderate temperatures.[13] Our results did not allow an unambiguous identification of any intermetallics, partly due to the large number of overlapping substrate and rhenium peaks. It should also be pointed out that the Re–Al intermetallics identified in Ref. 13 were found after annealing times on the order of 30 h or more rather than the 30 min used in our study. It is possible that the amount of solid-state reaction products is sufficient to affect the electrical behavior while it remains below the detection limit of a bulk materials characterization technique such as XRD. On the other hand, our XRD data clearly shows that the Re film on AlGaN is highly textured. Upon annealing, crystallization and grain growth allows some peaks to become visible, similar to that observed in a Re/GaAs system.[4] It is also expected that stress relief will occur as the lattice parameter of Re is smaller than that of AlGaN. However, it is considered unlikely that these phenomena can account for the significant changes in electrical behavior seen from $I-V$ measurements. Another scenario which might also lead to shunt conduction and barrier degradation upon high-temperature annealing is metal migration along line defects such as a network of dislocations.[14] Additional transmission electron microscopy analysis is being carried out to study any possible metallurgical reactions and structural changes at the Re/AlGaN interface.

In conclusion, we have presented the Schottky characteristics of refractory metal rhenium on n-$Al_xGa_{1-x}N$ after high-temperature annealing. The barrier height increases initially but drops off after annealing at 600 °C. $I-V-T$ analysis clearly shows the existence of shunt conduction pathways associated with the observed barrier degradation. In addition, DLTS analysis shows a new defect level at 0.34 eV below E_c after annealing. Further studies are needed to ascertain if structural degradation or hopping conduction through defect levels are responsible for the observed low-bias current anomaly.

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Thermally-stable low-resistance Ti/Al/Mo/Au multilayer ohmic contacts on $n-GaN$

V. Kumar, L. Zhou, D. Selvanathan, and I. Adesida
Department of Electrical and Computer Engineering and Micro and Nanotechnology Laboratory, University of Illinois at Urbana Champaign, Urbana, Illinois 61801

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A metallization scheme consisting of Ti/Al/Mo/Au with excellent edge acuity has been developed for obtaining low-resistance ohmic contacts to $n-GaN$. Excellent ohmic characteristics with a specific contact resistivity as low as $4.7\times10^{-7}\,\Omega\text{-cm}^2$ were obtained by rapid thermal annealing of evaporated Ti/Al/Mo/Au at 850 °C for 30 sec in a N_2 ambient. Additionally, no degradation in specific contact resistivity was observed for these contacts subjected to long-term annealing at 500 °C for 360 h. © *2002 American Institute of Physics.* [DOI: 10.1063/1.1491584]

The GaN-based material system is of great interest not only for blue/green light-emitting diodes, laser diodes, and UV photodetectors, but also for realization of high-frequency and high-power electronic devices at elevated temperatures.[1–3] This is due to its unique material properties such as a wide band gap leading to high-breakdown fields, a high-electron saturated velocity resulting in high speed, and the existence of AlGaN/GaN heterostructure with a high-conduction band offset and high piezoelectricity resulting in high-sheet carrier densities in the $1.0\times10^{13}\,\text{cm}^{-2}$ range. However, among the various problems limiting the performance of these devices are the need to form ohmic contacts with very low resistance, smooth morphology, and good edge acuity, and thermal stability for reliable high-temperature performance. These factors are critical to the fabrication of short channel electronic devices, namely, high-electron mobility transistors (HEMTs) and metal-semiconductors field effect transistors (MESFETs). A wide variety of ohmic contacts have been reported for $n-GaN$. Among them, the Ti/Al bilayer metal system has been the most commonly adopted contact on $n-GaN$.[4–8] Rapid thermal annealing at a temperature as high as 900 °C in N_2 or Ar ambient is widely used to alloy these bilayer contacts. However, due to the low-melting point of Al together with its propensity to oxidize at elevated temperatures, these contacts have severe reliability limitations when subjected to high-temperature processing, or when operating under high-temperature conditions. To avoid this propensity of oxidation at elevated temperatures, Ni/Au was added on top of this bilayer to obtain a Ti/Al/Ni/Au contact.[9] A very low-specific contact resistivity of $3.6\times10^{-8}\,\Omega\text{-cm}^2$ was achieved on reactively ion-etched $n-GaN$. Results on other metal composites such as Ti/Al/Ti/Au, Ti/Al/Pd/Au, and Ti/Al/Pt/Au have also been reported.[10–14] In general, higher-melting-point metals exhibit lower-bulk diffusivities.[15] Mo has a significantly higher-melting point than either Ni or other potential diffusion barriers such as Ti, Pd, and Pt. Also, binary phase diagrams show that Au has less than 1% solubility in Mo at the contact annealing temperature in the range of 850 °C, while its solubility in Ti and Pt are significantly higher, and reaching 100% in Ni and Pd. Hence, it will be of great interest to investigate the performance of the Ti/Al/Mo/Au metallization scheme, where Mo is the diffusion barrier between Al and Au.

The epitaxial layer used in the present study was grown on *c*-face sapphire substrates by metal-organic chemical-vapor deposition. The epilayer consisted of an AlN buffer, a 1 μm undoped GaN and a 1 μm Si-doped $n-GaN$. Hall measurements indicated a bulk carrier concentration of $1\times10^{18}\,\text{cm}^{-3}$ and mobility of about 250 cm^2/volt-sec at room temperature. Mesas for transmission line measurements were etched using Cl_2/Ar plasma in an inductively coupled-plasma reactive ion etch (ICP-RIE) system. Next, rectangular pads were patterned on these electrically isolated mesas, and a Ti/Al/Mo/Au (15 nm/60 nm/35 nm/50 nm) composite was evaporated on the mesas. Electron-beam evaporation was used to deposit Ti, Al, and Mo, while Au was deposited by thermal evaporation. Also, a pretreatment of the ohmic contact area using $SiCl_4$ plasma in a RIE system was performed prior to metallization.[16] Rapid thermal annealing of the samples was performed in an N_2 ambient. On-wafer current-voltage measurements were performed at room temperature using a HP4142B semiconductor analyzer. Four probes were used to eliminate the effects of resistance between the probes and metal contacts. The specific contact resistivity was extracted from a linear curve fit of the measured resistance versus gap spacing plot.

The $I-V$ characteristics for the as-deposited and annealed contacts, measured between ohmic pads with a spacing of 2 μm are shown in Fig. 1. The as-deposited contacts are ohmic. However, it is interesting to note that annealing at 500 °C results in rectifying behavior. Similar behavior has been observed for the Ti/Al/Ni/Au metallization.[17] This rectifying characteristic is attributed to the formation of an initial phase of TiN. This initial phase of TiN probably forms a heterojunction or a quasi-metal-insulator-semiconductor structure resulting in a higher-barrier height. Annealing at higher temperatures results in diffusion of Al through Ti to reach the $n-GaN$ surface. Al then reacts with the GaN surface to form a thin AlN layer at the interface, or a Ti–Al–N phase with a more favorable work function. The process of formation of both TiN and AlN results in creation of N va-

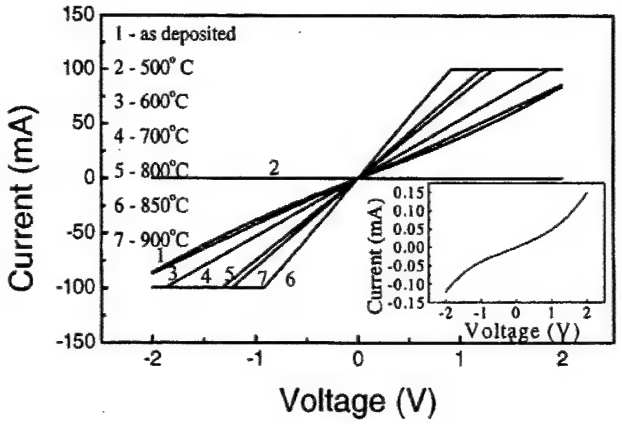


FIG. 1. Current-voltage characteristics of Ti(15 nm)/Al(60 nm)/Mo(35 nm)/Au(50 nm) contacts on $n-$GaN for the as-deposited and after annealing at various temperatures for 30 s. Inset: current-voltage characteristics after annealing at 500 °C for 30 s.

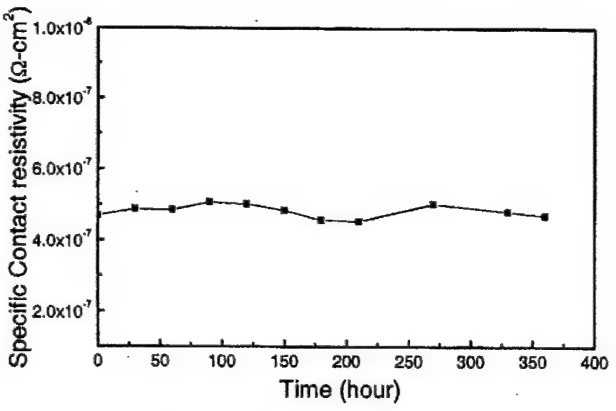


FIG. 3. Specific contact resistivity as a function of aging time (T_{aging} = 500 °C) of a Ti(15 nm)/Al(60 nm)/Mo(35 nm)/Au(50 nm) contacts on $n-$GaN annealed for 30 s.

cancies, which yields a heavily doped interface, resulting in a tunneling current responsible for ohmic contact formation.[5] The presence of a thin AlN layer has been experimentally confirmed by high-resolution transmission electron microscopy and electron energy dispersive x-ray spectroscopy at the interface of Ti/Al and Pd/Al contacts on $n-$GaN.[18] The variation of specific contact resistivity as a function of anneal temperature is shown in Fig. 2. As can be seen, the specific contact resistivity decreases steadily with the increase of annealing temperature up to 850 °C. Further increase of the anneal temperature results in a slight increase of specific contact resistivity. A specific contact resistivity as low as $4.7\times10^{-7}\ \Omega\text{-cm}^2$ has been obtained at an anneal temperature of 850 °C.

To ensure the suitability of Ti/Al/Mo/Au for high-temperature and high-power applications, these contacts were subjected to long-term thermal annealing treatment. No degradation of contact resistance was observed even after annealing these contacts at 500 °C for 360 hours as shown in Fig. 3. This implies that the Mo/Au layers protected the Al layers against oxidation, and that the Mo layer prevented diffusion of Au through the Ti/Al layers to degrade the contacts. In order to guarantee a good contact pattern definition, the contact surface morphology must be smooth. An atomic force microscope image of the as-deposited and annealed Ti/Al/Mo/Au (15 nm/60 nm/35 nm/50 nm) contact on $n-$GaN at 850 °C is shown in Figs. 4(a) and 4(b), respectively. The root-mean-square values for the surface roughness of the as-deposited and annealed contacts are 1 and 17 nm, respectively. The value of surface roughness for the annealed contacts is lower than previously reported values for Ti/Al/Ni/Au contacts.[17,19] Figure 5 is a scanning electron mi-

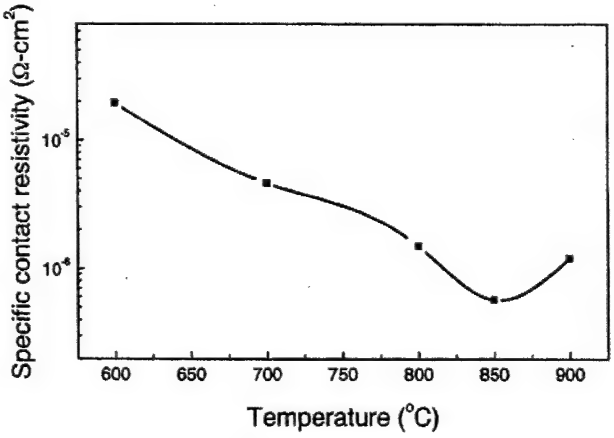
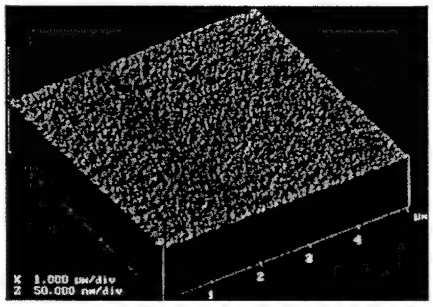
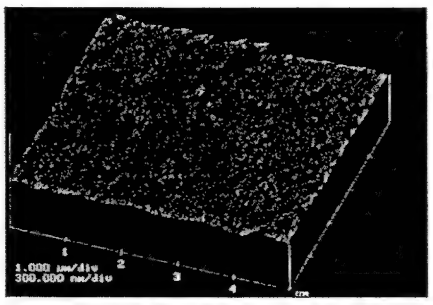


FIG. 2. Specific contact resistivity as a function of annealing temperature of Ti(15 nm)/Al(60 nm)/Mo(35 nm)/Au(50 nm) contacts on $n-$GaN annealed for 30 s.



(a) as-deposited



(b) annealed

FIG. 4. AFM micrographs of the Ti/Al/Mo/Au ohmic contacts (a) before and (b) after annealing at 850 °C for 30 s.

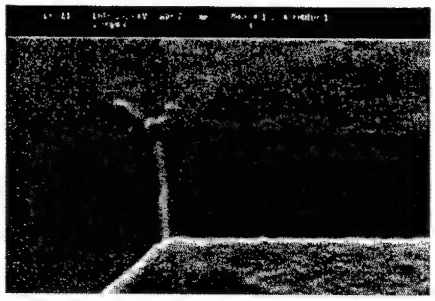


FIG. 5. Edge acuity of the annealed (850 °C for 30 s) Ti/Al/Mo/Au ohmic contact (source-drain spacing=2 μm).

croscopy (SEM) micrograph showing the smooth surface quality and excellent edge acuity of the ohmic contact.

In summary, a metallization scheme Ti/Al/Mo/Au was developed to form low-resistance ohmic contacts with excellent edge acuity on $n-$GaN. A specific contact resistivity as low as $4.7\times10^{-7}\ \Omega\text{-cm}^2$ has been achieved on moderately doped $n-$GaN. Also, the surface morphology of the annealed contact was smooth. No degradation in contact resistance was observed when these contacts were subjected to long-term annealing at 500 °C for 360 h. These features make Ti/Al/Mo/Au contacts very attractive for use as ohmic metallization in the fabrication of short-channel HEMTs and MESFETs. Detailed studies on the Ti/Al/Mo/Au interactions with GaN are in progress.

ACKNOWLEDGMENTS

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If the power MOSFET is controlling a clamped inductive load, the rise of drain current on turn-on occurs before the fall in drain voltage so that the current transformer is less effective in this case in reducing the MOSFET turn-on time. However, a fast turn-on is often not required in the case of a clamped inductive load since since this results in an unacceptably large value of diode recovery current. With insulated gate bipolar transistors other considerations apply but some advantage in reducing turn-on time with a resistive load has been observed.

Conclusion: It has been demonstrated that the turn-on time of a power MOSFET can be reduced, for a given set of gate drive conditions, by the inclusion in the drain lead of a small current transformer in the drain lead. Energy withdrawn from the gate circuit by the Miller capacitance is replaced by energy obtained from the change of flux in the transformer core. The transformer is sufficiently small to be able to allow it to be fabricated as part of the packaged MOSFET. The incorporation of this feature in power MOSFETs would permit the use of lower voltage, lower power gate driver circuits.

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D.A. Grant (*Department of Electrical and Electronic Engineering, University of Bristol, Merchant Venturers Building, University Walk, Bristol BS8 1TR, United Kingdom*)

E-mail: Duncan.Grant@bris.ac.uk

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Ohmic contacts on *n*-type $Al_{0.59}Ga_{0.41}N$ for solar blind detectors

D. Selvanathan, L. Zhou, V. Kumar, J.P. Long, M.A.L. Johnson, J.F. Schetzina and I. Adesida

Low-resistance ohmic contacts on $Al_{0.59}Ga_{0.41}N$ were formed using a Ti/Al/Mo/Au metallisation scheme. A specific contact resistivity as low as 6×10^{-5} Ω-cm^2 was achieved using a pre-metallisation treatment of the surface in an $SiCl_4$ plasma with a self-bias voltage of −300 V in a reactive ion etching system.

Wide bandgap $Al_xGa_{1-x}N$ is the material of choice in the development of the ultraviolet (UV) photodetectors with visible or solar-blind properties. These devices are of importance in solar-UV monitoring, space communications, missile detection and flame and heat sensing applications. For the fabrication of solar-blind UV photodetectors with a sharp transmission cutoff wavelength at $\lambda < 280$ nm, Al mole fraction $x \geq 0.4$ is required in the $Al_xGa_{1-x}N$ material system. Formation of good quality ohmic contacts with low resistance and smooth morphology is a requisite for the fabrication of highly efficient UV detectors. Previously, ohmic contacts to *n*-AlGaN were formed using the Ti/Al [1] and Ti/Al/Ti/Au [2] metallisations. The specific contact resistivity of Ti/Al/Ti/Au ohmic contacts on $Al_{0.40}Ga_{0.60}N$ was reported to be 2.5×10^{-3} Ω-cm^2 [2]. The performance of these devices is limited by the high contact resistance of the ohmic contacts. Recently, we have established low resistance, thermally-stable ohmic contacts on *n*-GaN using a metallisation scheme consisting of Ti/Al/Mo/Au. In this Letter, we report a low-resistance ohmic metallisation for $Al_{0.59}Ga_{0.41}N$ layer using pre-metallisation treatment of the surface with $SiCl_4$ plasma reactive ion etching [3]. We study the resistance and specific contact resistivity of the ohmic contacts against the pre-metallisation $SiCl_4$ plasma etch self-bias voltage.

The epitaxial layer was grown using metal organic chemical vapour deposition (MOCVD) on a *c*-face sapphire substrate. The epilayer consisted of an AlN buffer, a 1 μm unintentionally doped GaN and a 0.25 μm *n*-type $Al_{0.59}Ga_{0.41}N$ with a doping concentration of 3×10^{17} cm^{-3} as determined by capacitance-voltage measurements at 1 MHz. The Al mole fraction of 59% was established by cathodoluminescence measurements. The layers were degreased and sonicated to remove organic contaminants from the surface. Mesas were etched using Cl_2/Ar plasma in an inductively-coupled-plasma reactive ion etch (ICP-RIE) system to electrically isolate the various transmission line measurements (TLM) structures. Next, the ohmic contact pads were patterned using optical lithography. Prior to metallisation the surfaces were treated using $SiCl_4$ plasma in a reactive ion etching (RIE) system followed by a HCl:H_2O rinse to remove any surface oxide layer. Thereafter, an ohmic metallisation consisting of Ti (15 nm)/Al (60 nm)/Mo (35 nm)/Au (50 nm) was deposited. Ti, Al and Mo were electron-beam evaporated while Au was thermally evaporated. The TLM ohmic pads were delineated using a lift-off process and the gap spacing between the TLM contacts were 2, 3, 4, 5, 6, 8 and 10 μm, respectively. The ohmic contacts were alloyed at 850°C for 30 s in an N_2 ambient using a rapid thermal annealing (RTA) furnace. Current-voltage (I–V) measurements were made at room temperature using an HP4142B semiconductor parameter analyser. The I–V characteristics of the annealed ohmic contacts on untreated and plasma-treated surfaces for a gap spacing of 5 μm are shown in Fig. 1. The ohmic contacts on plasma-treated surfaces exhibit better I–V characteristics than those on untreated surfaces, while the as-deposited ohmic contacts on untreated surfaces exhibit rectifying behaviour.

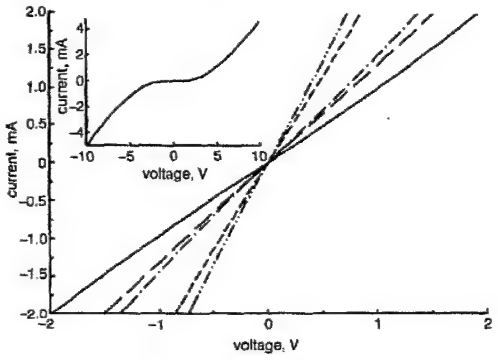

Fig. 1 *I–V characteristics of annealed ohmic contacts on untreated surface and on $SiCl_4$ plasma-treated surfaces for gap spacing of 5 μm*

Contacts annealed at 850°C for 30 s
——— untreated
– – – plasma voltage −100 V
——— plasma voltage −200 V
--------- plasma voltage −300 V
—·—·— plasma voltage −400 V
Inset: as-deposited ohmic contacts on untreated surface exhibiting rectifying behaviour

The contact resistance is extracted from a linear curve fit of the measured resistance against gap spacing plot for various pre-metallisation plasma etch bias voltages and a typical plot is shown in Fig. 2. The *y*-intercept and the slope determine contact resistance (R_c) and sheet resistance (R_s), respectively. The value for specific contact resistivity (ρ_c) is calculated from R_c and the *x*-intercept. The variation of contact resistance and specific contact resistivity of the annealed ohmic contacts on plasma-treated surfaces against plasma self-bias voltage is shown in Fig. 3. The TLM results indicate that the contact resistance of the ohmic contacts decreases monotonically from 48 to 6 Ω-mm as the plasma self-bias voltage is increased from 0 to −300 V and thereafter remains constant as the plasma self-bias voltage is increased to −400 V. The specific contact resistivity of the Ti/Al/Mo/Au ohmic contacts exhibits a similar characteristic with a minimum value of 6×10^{-5} Ω-cm^2 for the surface treated with a plasma self-bias voltage of −300 V. This value is over an order of magnitude lower than that previously reported for Ti/Al/Ti/Au ohmic contact on $Al_{0.40}Ga_{0.60}N$ layer [2]. The sheet resistance decreases from 20 KΩ/sq. in the untreated surface to a minimum of 6 KΩ/sq. in the $SiCl_4$ plasma-treated surface at a self-

bias voltage of −300 V and thereafter is constant as the plasma bias-voltage is increased to −400 V. Prolonged exposure of the ohmic contacts to the atmosphere did not degrade the ohmic performance. The root mean square (rms) values of the surface roughness of the as-deposited and annealed ohmic contacts measured using an atomic force microscope (AFM) are 2 and 35 nm, respectively.

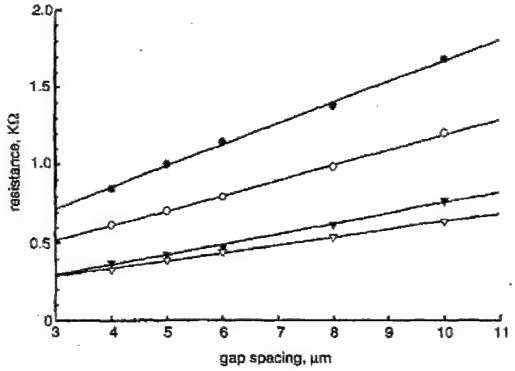

Fig. 2 *Measured resistance against TLM gap spacing for Ti/Al/Mo/Au contacts annealed at 850°C for 30 s*

Etching conditions were 25 mT and 10 sccm $SiCl_4$ for 1 min
plasma voltage −100 V
○ plasma voltage −200 V
▼ plasma voltage −300 V
▽ plasma voltage −400 V

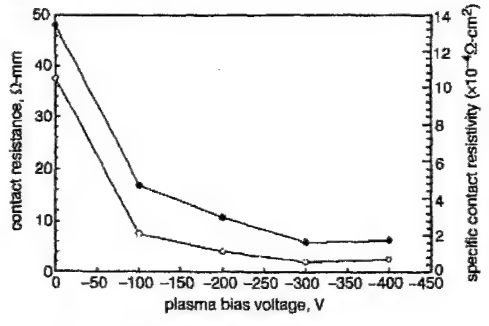

Fig. 3 *Contact resistance and specific contact resistivity against pre-metallisation $SiCl_4$ plasma etch self-bias voltage of Ti/Al/Mo/Au contacts annealed at 850°C for 30 s*

— contact resistance
–○– specific contact resistivity

Conclusion: We have developed an ohmic metallisation scheme consisting of Ti/Al/Mo/Au to form low-resistance contacts on n-$Al_{0.59}Ga_{0.41}N$. A specific contact resistivity as low as 6×10^{-5} Ω-cm^2 was achieved using a pre-metallisation treatment of $SiCl_4$ plasma with a self-bias voltage of −300 V in an RIE system. These features make Ti/Al/Mo/Au ohmic metallisation very attractive for solar-blind UV detectors.

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D. Selvanathan, L. Zhou, V. Kumar and I. Adesida (*Micro and Nanotechnology Laboratory and the Department of Electrical and Computer Engineering, University of Illinois at Urbana Champaign, Urbana, IL 61801, USA*)

J.P. Long, M.A.L. Johnson and J.F. Schetzina (*Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, NC 27695, USA*)

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Hilbert transformed phase-splitting fractionally spaced equaliser

Kyu-Min Kang and Gi-Hong Im

A phase-splitting fractionally spaced equaliser (PS-FSE) with a Hilbert filter is proposed, and the convergence and steady-state behaviours are analysed. The proposed PS-FSE employs one real-valued adaptive filter, which utilises both in-phase and quadrature error signals for weight update. The initial convergence speed of the proposed PS-FSE is approximately twice faster than the conventional PS-FSE.

Introduction: A great variety of adaptive equaliser structures can be used for carrierless amplitude and phase modulation (CAP) signals [1]. For instance, all the types of equalisers that are used for quadrature amplitude modulation (QAM) can be used for CAP as well, except that CAP does not use the phase recovery circuit that is usually required at the output of the equaliser in a QAM implementation. For QAM signals, a complex-valued fractionally spaced equaliser (CFSE) can be used. An alternative FSE is phase-splitting FSE (PS-FSE), which directly uses the received real passband signal as its input [2]. Note that the PS-FSE consists of two real-valued adaptive filters, as compared to four real-valued adaptive filters in the CFSE, and is therefore very attractive for practical implementation. However, the convergence time of the PS-FSE is approximately twice longer than the CFSE [3]. In this Letter, we propose a so-called Hilbert transformed PS-FSE, which is a PS-FSE with a Hilbert filter. The proposed PS-FSE requires one adaptive filter, which utilises both in-phase and quadrature error signals for weight update. Thus, the convergence speed of the proposed PS-FSE is faster than the conventional PS-FSE, while the computational complexity of the proposed PS-FSE is similar to the conventional PS-FSE.

The conventional PS-FSE consists of two real-valued adaptive filters. It is possible that the two adaptive filters of the PS-FSE converge to wrong solutions when a blind algorithm is used at the initial start-up period. This may occur because a blind algorithm converges the two adaptive filters independently. As the proposed PS-FSE employs only one real-valued adaptive filter, the possible wrong solution does not occur in a blind start-up mode.

Convergence analysis of Hilbert transformed PS-FSE: In this Section, we investigate the convergence and steady-state behaviours of a Hilbert transformed PS-FSE, which employs the least mean square (LMS) adaptive filtering algorithm. We briefly explain the conventional PS-FSE, and then propose a new equaliser structure. The analyses of minimum mean square error (MSE) and the optimum tap coefficients of conventional phase-splitting equalisers are given in [1]. For adaptation of the conventional PS-FSE taps, the LMS algorithm, which updates the tap coefficients in the opposite direction from the noisy error gradient, is used as follows:

$$\mathbf{c}_{I,n+1} = \mathbf{c}_{I,n} - \beta e_{I,n}\mathbf{r}_n$$
$$\mathbf{c}_{Q,n+1} = \mathbf{c}_{Q,n} - \beta e_{Q,n}\mathbf{r}_n$$

where

$$e_{I,n} = \mathbf{c}_{I,n}^T\mathbf{r}_n - s_{I,n-d} \quad \text{and} \quad e_{Q,n} = \mathbf{c}_{Q,n}^T\mathbf{r}_n - s_{Q,n-d}$$

$\mathbf{c}_{I,n}$ and $\mathbf{c}_{Q,n}$ denote the vectors of the in-phase and quadrature tap coefficients, respectively. $\mathbf{r}_n$ is the received real passband signal vector

Ion-beam processing effects on the thermal conductivity of *n*-GaN/sapphire (0001)

D. I. Florescu[a] and Fred H. Pollak[b,c]
Physics Department and New York State Center for Advanced Technology in Ultrafast Photonic Materials and Applications, Brooklyn College of CUNY, Brooklyn, New York 11210

William B. Lanford, Farid Khan, and I. Adesida
University of Illinois at Urbana-Champaign, Urbana, Illinois 61801

R. J. Molnar
Massachusetts Institute of Technology, Lincoln Laboratory, Lexington, Massachusetts 02420

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We have measured high spatial/depth resolution (2–3 μm) thermal conductivity (κ) at 300 K before and after plasma-induced effects on two series of *n*-GaN sapphire (0001) samples fabricated by hydride vapor phase epitaxy using scanning thermal microscopy. The sample thicknesses were 50 ± 5 μm for one set and 25 ± 5 μm for the second. The carrier concentrations were $\sim 8 \times 10^{16}\,\mathrm{cm}^{-3}$ and $\sim 1.5 \times 10^{17}\,\mathrm{cm}^{-3}$, respectively, as determined by Hall effect measurements. The thermal conductivity before treatment was similar to that previously reported for hydride vapor phase epitaxy material with comparable carrier concentration and thickness [D. I. Florescu *et al.*, J. Appl. Phys. **88**, 3295 (2000)]. Damage was induced by ion-beam processing the samples under constant Ar^+ gas flow and pressure for a fixed period of time (5 min), with the dc bias voltage (V_{dc}) being the only variable processing parameter (125–500 V). The thermal conductivity near the surface, κ, was found to exhibit a linear decrease with V_{dc} in the investigated range after this procedure. A second process was then applied in order to remove some damage. In this case the samples were processed under a constant mixture of Cl_2 and Ar^+ gas flow and V'_{dc} of 50 V. For the samples with V_{dc} in the range $125\,\mathrm{V} < V_{dc} \leqslant 250\,\mathrm{V}$, κ was found to be actually lower after the damage removal process. The minimum κ was found at 250 V. This is probably due to Ar^+ beam channeling [O. Breitschadel *et al.*, Appl. Phys. Lett. **76**, 1899 (2000)], which has been reported on similar structures at this voltage. When the initial processing voltage was $250\,\mathrm{V} < V_{dc} < 500\,\mathrm{V}$, κ showed a tendency to recover somewhat. © *2002 American Institute of Physics.*
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I. INTRODUCTION

Ion beams are broadly used in the semiconductor industry for a wide range of processing steps, such as dry etching, dopant implantation, implant isolation, and material characterization.[1] Lattice induced disorder is commonly found to be a side effect of the ion bombardment. Up to date relatively few studies have been reported on ion-beam induced damage in GaN.[2–4] GaN (and other group III-nitride semiconductors) has attracted considerable attention in recent years for utilization in high power optoelectronic and electronic devices, including blue/green light emitting diodes (LED), lasers, and solid-state transistors.[5–8] These high power/high temperature applications make thermal behavior, particularly the thermal conductivity (κ), an extremely important material property. The substrate's ability to dissipate heat directly affects its device performance. The thermal conductivity of solid materials consists of both lattice and electronic contributions. The former is a function of the mean free path of the phonons and hence is determined by both intrinsic (anharmonic phonon-phonon scattering) and extrinsic (phonon-defect) effects. The presence of generic defects (point, extended, process-induced, etc.) lowers the thermal conductivity. For carrier concentrations $\leqslant 10^{19}\,\mathrm{cm}^{-3}$ the electronic thermal conductivity is negligible in relation to the lattice portion. The quantity κ is of importance from both fundamental (basic mechanism of phonon propagation) and applied (device modeling, sample quality) perspectives. However, despite the considerable body of work, both experimental and theoretical, on the electronic, optical, and structural properties of the group III-nitride semiconductors relatively few investigations have been reported on thermal conductivity measurements[9–16] or theory.[17–19]

This paper will discuss the thermal conductivity behavior before and after inductively coupled plasma processing on two series of hydride vapor phase epitaxy (HVPE) *n*-GaN/sapphire (0001) samples. The influence of damage and removal on κ is likely to be extremely important for plasma-processed devices and their thermal modeling. Certain GaN applications, such as blue/green LEDs, lasers, and solid-state transistors, would benefit greatly from GaN with

[a]Present address: Emcore Corporation, 145 Belmont Drive, Somerset, NJ 08502.
[b]Also at the Graduate School and University Center of the City University of New York, New York, NY 10016.
[c]Electronic mail: fhpbc@cunyvm.cuny.edu

higher thermal conductivity, as heat extraction from the device becomes more efficient with higher κ. Thus information on the effects of the technological processing steps affecting the device's performance is an important design consideration.

II. EXPERIMENTAL DETAILS

The GaN samples used in this study were grown by the HVPE method in a vertical-type reactor.[20] A more extensive description of the growth procedure and parameters is presented in Refs. 12 and 14. Four 5 mm×5 mm pieces were cut from two different wafers and labeled set A and set B. For set A the film thicknesses were 50 ± 5 μm with $n\sim8\times10^{16}\,\mathrm{cm}^{-3}$, as determined by Hall effect measurements. The high spatial/depth resolution (2–3 μm) κ measurements were made using a ThermoMicroscope's AutoProbe M5 SThM system.[21] A calibration method has been developed making possible the use of this instrument for the evaluation of absolute values of κ,[10,12,16] i.e., with the thermoresistive tip in feedback the square of the instrument output voltage is proportional to the thermal conductivity of the specimen in the calibrated range.

A Unaxis SLR (shuttlelock ready) inductively coupled plasma (ICP)-reactive ion etching (RIE) system was used for the plasma processing of the samples. ICP-RIE is a versatile technique, which is characterized by both high plasma density ($>10^{11}\,\mathrm{cm}^{-3}$) and low chamber pressure operation (<10 Pa). Both the plasma density and substrate bias voltage can be controlled independently of the chamber pressure. Operation at low pressure typically aids directionality of the ion flux in an ICP-RIE system. Normal incidence was used for both damage and damage removal procedures. During the 5 min long damage-inducing phase, the ICP coil power was 500 W, the chamber pressure was 5 Pa, with 15 sccm Ar^+ gas flow. The only variable processing parameter was V_{dc}, which was adjusted to 125, 250, 375, and 500 V for the four pieces from each set. For the five minute damage removal procedure the ICP coil power was 300 W, the chamber pressure was 3 Pa, with 15 sccm Cl_2 gas flow in mixture with 5 sccm Ar^+ gas flow, and V'_{dc} was 50 V. The estimated depth of removed film was about 70 nm for set A and 100 nm for set B, as measured by a control sample. The damage depth is unknown.

III. EXPERIMENTAL RESULTS

A. Damage inducing procedure

Before treatment the thermal conductivity was measured to be 1.75 ± 0.10 W/cm K for set A, and 1.82 ± 0.12 W/cm K for set B. These values are similar to the thermal conductivity of HVPE GaN material with comparable carrier concentration and thickness.[14]

Plotted in Figs. 1(a) and 1(b) are κ measured after each individual damage inducing procedure as a function of V_{dc} on sets A and B, respectively. Representative error bars are shown. The solid lines in Figs. 1 are least-square fits to a linear function with the slopes being $\sim0.28\times10^{-3}/0.22\times10^{-3}$ W/cm K V for A/B. The thermal conductivity exhibits a linear decrease with the processing voltage in the investigated range on both sets. At 125 V, κ was only slightly less than the untreated case for set A (~1.65 W/cm K), but exhibited a somewhat larger drop for set B (~1.51 W/cm K). For the 500 V situation κ had dropped to ~0.5 W/cm K for set A and ~0.75 W/cm K for set B. Table I summarizes κ before and after the damage inducing procedure.

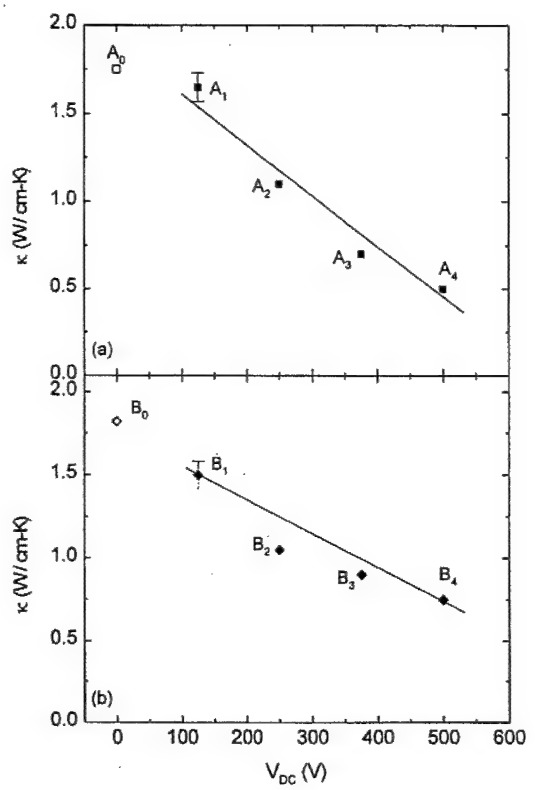

FIG. 1. Thermal conductivity before (open symbol) and after (solid symbol) the damage inducing procedure as a function of the processing voltage of (a) set A, and (b) set B. Representative error bars are shown. The solid lines are the least-square fits to a linear function.

B. Damage removal procedure

Shown in Figs. 2(a) and 2(b) are κ measured after the damage removing phase on sets A and B, respectively. Representative error bars are shown. The solid lines are guides to the eye. For samples initially processed at 125 V and 250 V the recorded κ are actually lower than the values measured

TABLE I. Summary of V_{dc} and κ on sets A and B before (A_0, B_0) and after the damage inducing procedure.

Sample	V_{dc}(V)	κ(W/cm K)
A_0	0	1.75±0.10
A_1	125	1.65±0.08
A_2	250	1.10±0.09
A_3	375	0.70±0.05
A_4	500	0.50±0.03
B_0	0	1.82±0.12
B_1	125	1.50±0.07
B_2	250	1.05±0.08
B_3	375	0.90±0.06
B_4	500	0.75±0.04

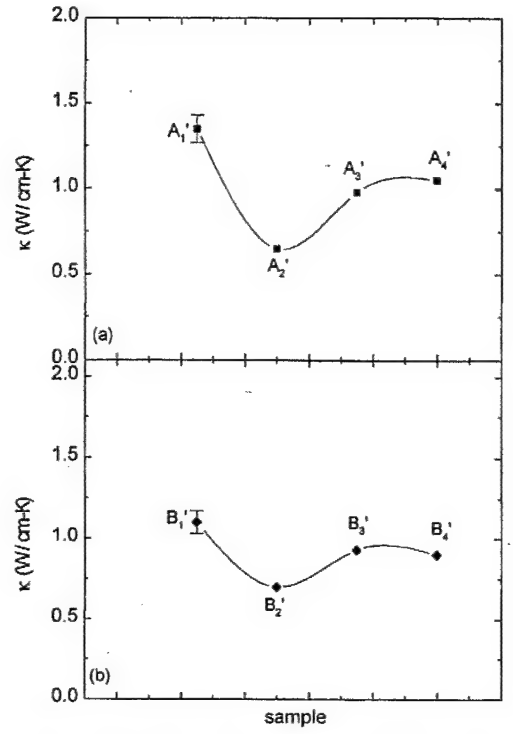

FIG. 2. Thermal conductivity after the damage removing procedure of (a) set A, and (b) set B. Representative error bars are shown. The solid lines are guides to the eye.

after the damage inducing procedure. The further drop is about 18%–20% for the samples processed at 125 V and 30%–40% for 250 V. The samples initially processed at 375 V and 500 V show improvement in their thermal conductivity values, but not full recovery. The highest κ jump is observed for sample four of set A from $\kappa_{\text{after-damage}} \sim 0.5$ W/cm K to $\kappa_{\text{after-removal}} \sim 1.05$ W/cm K. Table II summarizes κ after the damage removal procedure.

IV. DISCUSSION OF RESULTS

A theoretical prediction for the thermal conductivity of GaN at room temperature was initially estimated by Slack to be ~1.7 W/cm K.[17] A simple expression to calculate the thermal conductivity of perfect dielectric crystals at "high temperatures" (>120 K) was derived by Witek.[18] Using this approximation Witek estimated the room temperature thermal conductivity of GaN to be ~4.10 W/cm K. Subsequently Berman confirmed this value by evaluating the 300 K thermal resistivity of GaN.[19]

From kinetic theory the lattice thermal conductivity (κ_{lattice}) is given by[22]

$$\kappa_{\text{lattice}}(T) = (1/3) v_s c_{\text{lattice}}(T) l(T), \tag{1}$$

where v_s is the average velocity of sound (with only a weak temperature dependence), $c_{\text{lattice}}(T)$ is the lattice specific heat, and $l(T)$ is the phonon mean free path. At low temperatures, extrinsic effects such as "defects" and/or finite crystal size dominate l. With increasing temperature (a) $c_{\text{lattice}}(T)$ increases and then saturates when $T/\Theta_D \sim 0.5$, where Θ_D is the Debye temperature (~600 K for GaN[23]) and (b) intrinsic temperature dependent Umklapp processes become dominant, thus causing a decrease in l. This behavior is characteristic for semiconducting and insulating materials.[22] The maximum thermal conductivity (κ_{max}) is reached at some characteristic temperature T_{ch}, where for GaN $T_{\text{ch}} \sim 200$ K.[10] Since at 300 K we are close to T_{ch} for GaN, the thermal conductivity still has a strong dependence on extrinsic as well as intrinsic factors.

After the damage inducing procedure, the observed linear decrease of κ at room temperature with increasing V_{dc} could be attributed to a decrease in l associated with additional "defects" being created by the increasing bias voltage. In the case of the damage removal procedure, material is being removed without appreciable additional defects being generated, although the incomplete recovery of κ may be an indication of either residual damage from the first processing step or additional damage introduced in the etch step. For samples initially processed at voltages $\leqslant 250$ V the defects generated by the damage inducing beam lie deeper compared to the samples for which $V_{\text{dc}} > 250$ V. By removing a thin (70–100 nm) surface layer the former could exhibit a drop in κ, while the latter may show improvement. The defects generated for a processing voltage of 250 V could be the deepest under the abovementioned processing conditions.

Breitschadel *et al.*[24] investigated the effects of Ar ion-beam channeling on AlGaN/GaN heterostructures during the ion-beam etching process by measuring the sheet resistance before and after processing. They used a constant dc bias voltage of 250 V, and various angles of beam incidence. The sheet resistance is proportional to the resistivity.[24] The ratio of the sheet resistance before and after etching was measured to be about 1/9 for normal incidence, clearly indicating that the electron mobility drops after the dry etching process. The effect was maximum at normal incidence, and vanished at incident angles $>40°$. They attributed this behavior to traps/defects in the upper regions of the layers, which were generated during ion-beam etching. A similar behavior could be exhibited by κ. The newly generated traps/defects may reduce l, and hence κ. Our experiments were performed at normal incidence, but with different ion-beam energies. Based on these studies the observed dip in κ after the damage removal procedure could be attributed to a channeling effect of the incident Ar ion beam. This effect occurs for dc bias voltages $125 \text{ V} < V_{\text{dc}} \leqslant 250$ V, and is highest at 250 V. Clearly more work needs to be done in this area.

TABLE II. Summary of κ on sets A and B after the damage removal procedure ($V'_{\text{dc}} = 50$ V).

Sample	κ(W/cm K)
A'_1	1.35±0.08
A'_2	0.65±0.04
A'_3	0.95±0.07
A'_4	1.05±0.08
B'_1	1.10±0.07
B'_2	0.70±0.05
B'_3	0.95±0.06
B'_4	0.90±0.06

V. SUMMARY

Using SThM we have measured high spatial/depth (2–3 μm) resolution room temperature thermal conductivity before and after plasma-induced effects on two series of n-GaN/sapphire (0001) samples fabricated by HVPE. Before treatment κ was measured and found to be similar to earlier results on HVPE GaN material with comparable carrier concentration and thickness. Damage was induced by processing the samples under constant Ar^+ gas flow and pressure for a fixed period of time, with the dc bias voltage being the only variable processing parameter (125–500 V). After this procedure, κ was found to exhibit a linear decrease with V_{dc} in the investigated range. In order to remove some of the induced damage, the samples were processed under a constant mixture of Cl_2 and Ar^+ gas flow and pressure for a fixed period of time. The dc bias voltage during this procedure was 50 V. In relation to its value as a result of the ion damage, after damage removal κ was found to actually decrease for the samples processed at $125\,V < V_{dc} \leqslant 250\,V$ and to increase, but not completely recover, for $250\,V < V_{dc} < 500\,V$. The minimum κ value was found for an initial damage processing voltage of 250 V. Ar^+ beam channeling may be responsible for this behavior.

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Low Resistance Ti/Al/Mo/Au Ohmic Contacts for AlGaN/GaN Heterostructure Field Effect Transistors

D. SELVANATHAN[1]), L. ZHOU, V. KUMAR, and I. ADESIDA[2]),

Micro and Nanotechnology Laboratory and Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Urbana, IL 61801, U.S.A.

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A metallization scheme consisting of Ti/Al/Mo/Au was utilized to develop low-resistance ohmic contacts to AlGaN/GaN heterostructure field effect transistors (HFET). A contact resistance as low as 0.20 Ωmm and a specific contact resistivity as low as 4.5×10^{-7} Ωcm^2 were obtained using a pre-metallization surface treatment with $SiCl_4$ plasma at a self-bias voltage of −300 V in a reactive ion etching (RIE) system. X-ray photoelectron spectroscopy (XPS) measurements of the $SiCl_4$ plasma-treated surface revealed an increase in the N vacancies thereby increasing the donor concentration at the surface. Also a blue shift of the peak energy of the Ga 3d photoelectrons was observed showing that the Fermi level moved closer to the conduction band at the surface of the AlGaN.

Introduction AlGaN/GaN heterostructure field effect transistors (HFET) are devices of interest in the development of high temperature/high power electronics at microwave frequencies. To achieve efficient, high performance devices with high transconductance and high saturation current, high quality ohmic contacts with contact resistances less than 0.5 Ωmm are essential. Ohmic contacts to AlGaN/GaN HFETs have generally been formed using Ti/Al metallization scheme [1–3]. In order to prevent or minimize the oxidation of the Al, the utilization of Ni/Au, Ti/Au, and Pt/Au overlays in the Ti/Al metallization have been reported [4–9]. Recently, we have reported a low resistance ohmic contact consisting of Ti/Al/Mo/Au metallization scheme on n-GaN [10]. These contacts exhibited excellent ohmic characteristics with a specific contact resistivity as low as 4.8×10^{-7} Ω cm^2 and were thermally stable at 500 °C for 350 h. In this paper, we report Ti/Al/Mo/Au ohmic contacts on AlGaN/GaN HFETs. Previously, it was shown that pre-ohmic metal deposition reactive ion etching (RIE) of n-GaN surface using $SiCl_4$ plasma improved the contact resistance of the ohmic contacts on n-GaN [11]. In this work, we report the effects of $SiCl_4$ RIE on AlGaN/GaN HFET layers using transfer length measurements (TLM). The $SiCl_4$ plasma-treated surfaces were profiled using X-ray photoelectron spectroscopy (XPS) to study the chemical bonding at the surfaces. We also report the performance of Ti/Al/Mo/Au ohmic contacts on AlGaN/GaN HFETs in terms of the contact resistances and specific contact resistivities.

Experiment The epitaxial layer was grown using metalorganic chemical vapour deposition (MOCVD) on a *c*-face sapphire substrate. The epilayer consisted of an AlN

[1]) e-mail: selvanat@uiuc.edu
[2]) Corresponding author; Phone: +1 217 333-3097; Fax: +1 217 244-6375; e-mail: iadesida@uiuc.edu

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buffer, a 1 μm unintentionally-doped GaN and a 250 Å n-type $Al_{0.20}Ga_{0.80}N$ with a doping concentration of 2×10^{18} cm^{-3}. The sheet carrier concentration and the mobility of electrons in the channel were 8.5×10^{12} cm^{-2} and 1100 cm^2 v^{-1} s^{-1}, respectively. The layers were degreased and sonicated to remove organic contaminants from the surface. Mesas were etched using Cl_2/Ar plasma in an inductively-coupled-plasma reactive ion etching (ICP-RIE) system to electrically isolate the various TLM structures. Next, ohmic contact pads were patterned using optical lithography. Prior to metallization, the surfaces were treated using $SiCl_4$ plasma for 60 s in a reactive ion etching (RIE) system at a chamber pressure of 25 mTorr, a $SiCl_4$ flow rate of 10 sccm, and a plasma self-bias voltage ranging from −100 to −400 V. Prior to loading the sample in an evaporation chamber, they were cleaned in a HCl:H_2O solution to remove any surface oxide layer. Thereafter, an ohmic metallization consisting of Ti (15 nm)/Al (60 nm)/Mo (35 nm)/Au (50 nm) was deposited. Ti, Al and Mo were electron-beam evaporated while Au was thermally evaporated. The TLM ohmic pads were delineated using a lift-off process and the gap spacings between the TLM contacts were 2, 3, 4, 5, 6, 8, and 10 μm, respectively. The contacts were alloyed at 850 °C for 30 s in a N_2 ambient using a rapid thermal annealing (RTA) furnace. Current–voltage (I–V) measurements were performed at room temperature using an HP4142B semiconductor parameter analyzer. XPS measurements were performed using a Kratos Axis ULTRA X-ray Photoelectron Spectroscopy system.

Results and Discussion The TLM measurements were performed on the AlGaN/GaN layers as a function of $SiCl_4$ plasma bias voltage. The contact resistance was measured from a linear curve fit of the measured resistance vs. gap spacing plot and the variations of contact resistance and specific contact resistivity of the annealed ohmic contacts on plasma-treated surfaces as functions of the plasma self-bias voltage are shown in Fig. 1. The contact resistance of the ohmic contacts decreases from 0.32 Ω mm in the untreated sample to a minimum of 0.23 Ω mm at a plasma bias voltage of −300 V and thereafter increases to 0.26 Ω mm as the plasma bias voltage was increased to −400 V. The specific contact resistivity of the ohmic contacts also exhibited a similar trend with a minimum value of 6.5×10^{-7} Ω cm^2 for samples treated at a plasma self-bias voltage of −300 V.

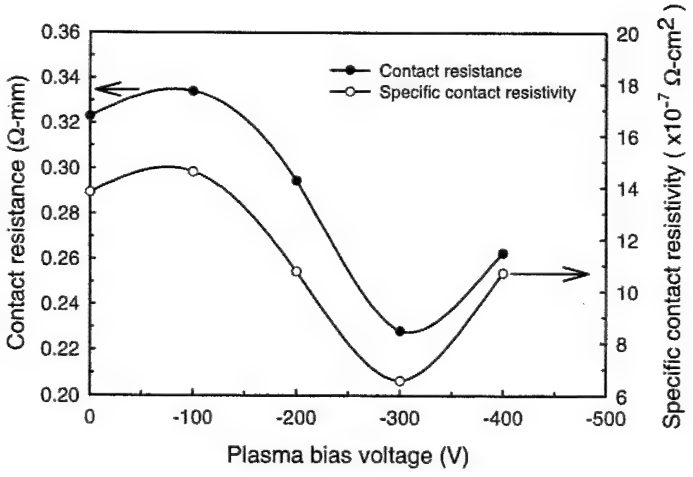

Fig. 1. Variations of contact resistance and specific contact resistivity of ohmic contacts on untreated and $SiCl_4$ plasma-treated AlGaN/GaN HFET layers. The conditions for the $SiCl_4$ plasma RIE treatment were 25 mTorr and 10 sccm $SiCl_4$ flow rate for 60 s and the ohmic contacts were annealed at 850 °C for 30 s in a N_2 ambient in a RTA furnace

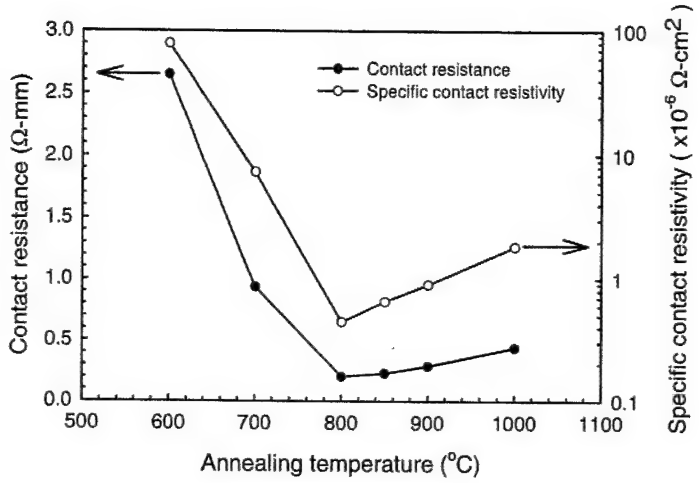

Fig. 2. Variations of contact resistance and specific contact resistivity as functions of rapid thermal annealing temperature. The samples were treated with $SiCl_4$ plasma at a bias voltage of −300 V. The ohmic contacts were annealed for 30 s in a N_2 ambient in a RTA furnace

To study the effects of anneal temperature on the contact resistance of the ohmic contacts, the AlGaN/GaN samples were treated using $SiCl_4$ plasma at a self-bias voltage of −300 V. Annealing was carried out at various temperatures ranging from 600–1000 °C for 30 s in N_2 ambient in a RTA furnace. Figure 2 shows the variations of contact resistance and specific contact resistivity of the ohmic contacts as functions of the anneal temperature. The TLM measurements indicate that contact resistance decreases from 2.7 Ω mm to a minimum of 0.20 Ω mm as the anneal temperature is increased from 600 °C to 800 °C and thereafter increases to 0.43 Ω mm as the temperature is increased to 1000 °C. The trend of the specific contact resistivity as a function of temperature is identical with a minimum value of 4.5×10^{-7} Ω cm^2 obtained at an anneal temperature of 800 °C.

Figure 3 illustrates the XPS spectra of Ga 3d photoelectrons taken at an angle of 30° to normal deviation. In samples treated with the $SiCl_4$ plasma, the peaks for the Ga-N bond indicate a blue-shift of 0.24 eV towards the higher binding energies with respect to the Ga-N bond on untreated samples. This suggests that the Fermi level, E_F, at the surface of the AlGaN moved near the conduction band edge due to the plasma treatment, resulting in the decrease of effective Schottky barrier height (SBH) for electron transport. Table 1 summarizes the ratio of the area under the Ga and Al peaks to that

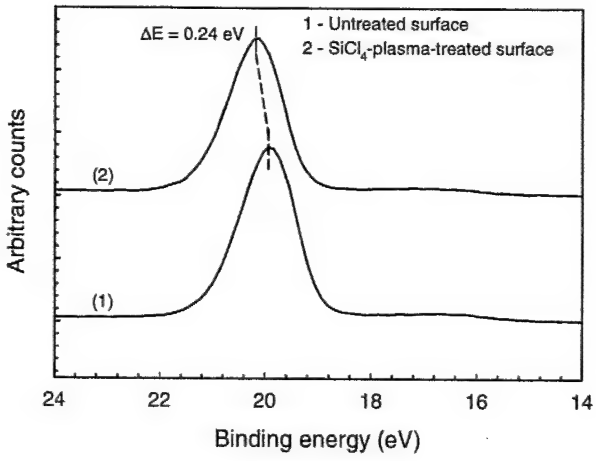

Fig. 3. XPS spectra of the Ga 3d photoelectrons at the surface of 1) untreated, and 2) $SiCl_4$ plasma-treated samples. The sample was treated with $SiCl_4$ plasma for 60 s at a self bias voltage of −300 V in a RIE system

Table 1
Summary of areas of Ga and Al peaks to N peak ratio from the XPS spectra of the surface in the untreated and $SiCl_4$ plasma-treated samples

surface treatment of sample	(Ga, Al)/N
untreated	0.5674
$SiCl_4$ plasma-treated	0.9242

of the N peak in the untreated and $SiCl_4$ plasma-treated samples. We find that the Ga and Al ratio to N increases in the $SiCl_4$ plasma-treated sample indicating an increase in N vacancies. This means that the N atoms predominantly escaped from the surface during the RIE treatment thereby effectively increasing the donor concentration at the surface. This leads to a higher electron concentration at the surface and thus effectively reducing the contact resistance of the ohmic contacts in the $SiCl_4$ plasma-treated samples.

Conclusions In conclusion, we have applied a novel metallization scheme consisting of Ti/Al/Mo/Au to develop low resistance ohmic contacts for AlGaN/GaN HFETs. A contact resistance as low as 0.20 Ω mm and a specific contact resistivity as low as 4.5×10^{-7} Ω cm^2 were achieved using a pre-metallization surface treatment with $SiCl_4$ plasma at a self-bias voltage of −300 V in a RIE system. The ohmic contacts were annealed at 800 °C in a N_2 ambient in a RTA furnace. These features make Ti/Al/Mo/Au ohmic contacts to AlGaN/GaN HFETS very attractive for high temperature/ high power electronic device applications.

Acknowledgements This work was supported by DARPA and by ONR under contract number N00014-01-1-1000 (monitor: Dr. J. Zolper).

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Ti-based Ohmic Contacts to *p*-Type GaN/$Al_xGa_{1-x}N$ Superlattices

I. Adesida*, L. Zhou, A. Osinsky[1], J.W. Yang[2] and M.A. Khan[2]

Microelectronics Laboratory, Department of Electrical and Computer Engineering, University of Illinois, Urbana-Champaign, IL 61801, U.S.A.
[1] *Corning Applied Technologies Corp., Woburn, MA 01801, U.S.A.,*
[2] *Department of Electrical and Computer Engineering, University of South Carolina, Columbia, SC 29208, U.S.A.*

Several metallization schemes were investigated as ohmic contacts to p-type GaN/$Al_xGa_{1-x}N$ short period superlattices (SL). Ti-based metallizations such as Ti/Pt/Au, deposited after conventional surface cleaning procedures, compare favorably with other ohmic contacts such as Ni/Au and Pd/Au deposited after the "two-step" surface treatments. Temperature-dependent transmission line measurements (TLM) show flat specific contact resistances (R_c) within the temperature range from -55 °C to 200 °C for the contacts used in this study, indicating field emission as the main conduction mechanism. Semiconductor sheet resistances obtained through the same measurement also demonstrate lowered dopant activation energies required for the SL, at approximately 60 meV for the GaN/$Al_{0.2}Ga_{0.8}N$ SL and 90 meV for the GaN/$Al_{0.1}Ga_{0.9}N$ SL, lower than the 200 meV required for p-GaN.

KYEWORD: Superlattices, Ohmic Contacts, Activation Energy, TLM, GaN, AlGaN, Surface, Sheet Resistance

1. Introduction

Rapid advances in the field of III-nitride device technology puts increasing demand on high performance ohmic contacts for both n-type and p-type materials. A number of different techniques utilized to obtain ohmic contacts on p-type GaN with specific contact resistances (R_c) on the order of 10^{-4} to 10^{-5} have been reported over the last year, including the use of GaN/$Al_xGa_{1-x}N$ short period superlattices (SL) or $In_xGa_{1-x}N$/GaN SL,[1-5] and using ultrasonic surface cleaning in buffered oxide etch (i.e., the so-called "two-step" surface treatment) prior to metal evaporation.[6] A significantly increased spatially averaged hole concentration in Mg-doped SL was observed with variable temperature Hall measurements.[3,5] On the other hand, Hall measurements and temperature dependent TLM analysis showed that prolonged cleaning in the "two-step" process may also significantly increase the concentration of carriers near the surface of p-GaN.[7] In this paper, we present results from temperature dependent TLM study of ohmic contacts fabricated using both conventional cleaning and the "two-step" surface treatment techniques.

2. Experimental

The superlattice layers used in this study were grown by molecular beam epitaxy on sapphire and consisted of 20 periods each of Mg-doped GaN (10 nm) and $Al_xGa_{1-x}N$ (10 nm). Samples with two different aluminum concentrations, x=0.1 and 0.2, were investigated. Both samples exhibited a mobility of ~1 $cm^2V^{-1}s^{-1}$ from room temperature Hall measurements. Actual Al mole fraction was confirmed by reciprocal space mapping using a Philips X'Pert high resolution X-ray diffractometer. The reference p-type GaN layer used in this study was grown using metalorganic chemical vapor deposition and has a 0.3 μm doped layer with a nominal bulk carrier concentration of $2.0x10^{17}$ cm^{-3} and a mobility of 9 $cm^2V^{-1}s^{-1}$ as obtained from Hall measurements at room temperature. Contact resistances were determined using the linear transfer length method (TLM). The structures used for the TLM measurements were fabricated by first patterning the p-GaN and SL samples with 100 x 650 μm mesas. The pattern was then transferred into the samples using reactive ion etching, which electrically isolated the mesas. Rectangular pads were then patterned. Prior to transferring the samples into the evaporation chamber, the surfaces were cleaned in O_2 plasma, followed by dips in a dilute HCl:DI (1:2) solution before metal deposition. "Two-step" surface treatments were used to prepare the surface for the deposition of metals other than Ti/Pt/Au. This treatment consists of a 10-minute ultrasonic clean in buffered oxide etch (BOE) prior to patterning, and a second BOE clean before metal evaporation. Electron beam evaporation was used to deposit Ti (15 nm) and Pt (50nm), while Au (80nm) was thermally evaporated as the last capping layer. In order to reduce experimental variables, all other bilayer metal contacts deposited contain 500 Å of the first contacting metal, plus an Au cap layer of 800 Å. Post-deposition heat treatment was carried out while flowing N_2 at 1 atmosphere in a rapid thermal annealing (RTA) system. The contact characteristics were studied using current-voltage (I-V) and four-probe linear TLM techniques at temperatures from -55 °C to 200 °C on a variable-temperature probe station equipped with an N_2-purged sample chamber.

3. Results and Discussions

Ni/Au is one of the most widely used ohmic contacts to p-type GaN and Fig. 1 shows the current-voltage (I-V) characteristics of Ni/Au (500 Å/800 Å) on the reference p-GaN and SL after annealing at 500 °C for 1 minute. In both cases, better linearity was observed in the I-V characteristics of the contact after prolonged ultrasonic cleaning in the BOE. The specific contact resistance (R_c) for the annealed Ni/Au contact was $3x10^{-4}$ Ω-cm^2 on the GaN/$Al_{0.2}Ga_{0.8}N$ SL after annealing.

R_c of bilayer ohmic contacts on GaN/$Al_{0.2}Ga_{0.8}N$ SL decreases with increasing metal work function of the first contacting layer. This dependence of R_c on metal work function can be seen in Fig. 2, which shows higher current at a given voltage for Pt/Au compared to other bilayer contacts, including the Ni/Au contact shown in Fig. 1, which is presented using the same scale. Rhenium was included in

* E-mail: iadesida@uiuc.edu

our study because it exhibits superior thermal stability compared to both Pd and Pt on GaN.[8] However, due to its lower work function of 5.0 eV, the I-V curve was slightly Schottky. In all cases, the bilayer contacts started to degrade at annealing temperatures higher than 550 °C; the temperatures were below those required for significant metallurgical reactions between GaN and these metals. One possible origin of this degradation is temperature-induced microstructural changes in the conductive near-surface layer created by the BOE etching.

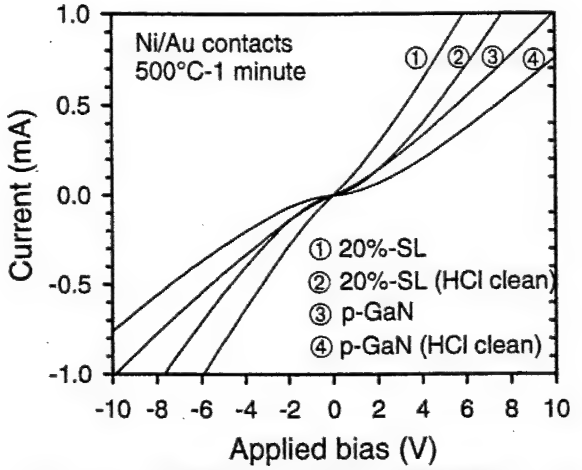

Fig. 1 I-V characteristics of Ni/Au (50nm/80nm) contacts after annealing for 500 °C for 1 minute. The sample surface was ultrasonically cleaned with BOE unless otherwise stated. 20%-SL represents GaN/$Al_{0.2}Ga_{0.8}$N-SL.

Fig. 2 also demonstrates the effectiveness of Ti/Pt/Au contact, which exhibits lower resistance than all of the bilayer metallizations investigated in this study. The low resistance with Ti/Pt/Au contact was achieved with only conventional cleaning of the sample surface, i.e., HCl dip prior to metal evaporation.

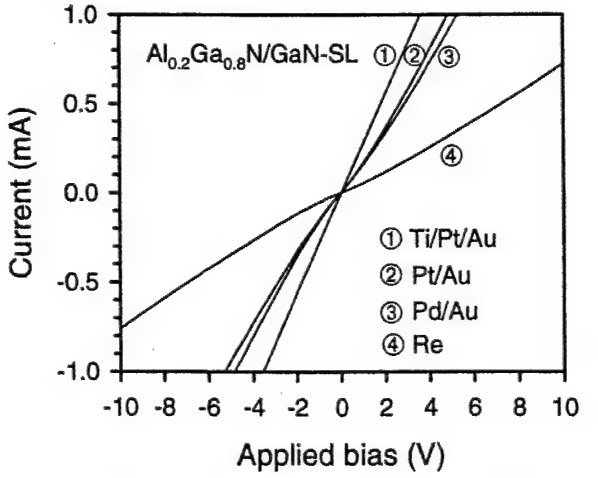

Fig. 2 Best I-V characteristics exhibited by different contacts on GaN/$Al_{0.2}Ga_{0.8}$N-SL after annealing. The surfaces were ultrasonically cleaned with BOE prior to photoresist patterning, except for Ti/Pt/Au.

Temperature-dependent TLM analysis was carried out to study the electronic transport mechanism of these contacts. The results are presented in Fig. 3, which plots the log (Rc) vs. 1000/T. An almost flat Rc over a wide temperature range from –55 °C to 200 °C is an indication that field emission is the dominant transport mechanism for these ohmic contacts on the SL. Based on the theory of metal-semiconductor contacts, field emission will dominate the current transport when the tunneling parameter satisfies the condition that $E_{00}/kT>>1$.

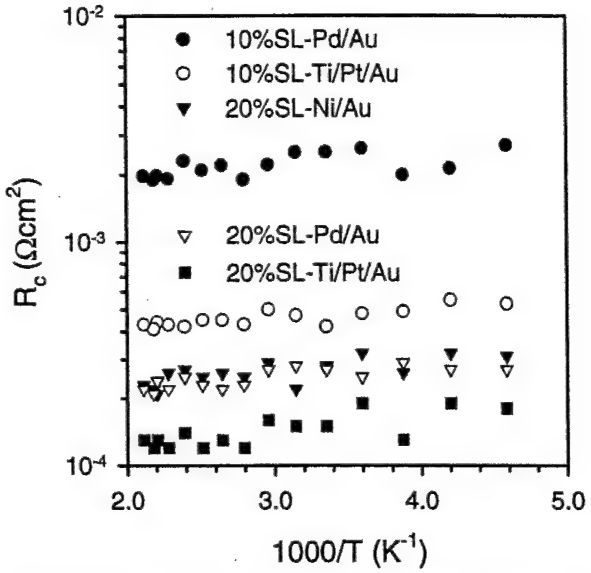

Fig. 3 Temperature-dependent TLM measurement of various contacts on GaN/Al_xGa_{1-x}N-SL.

The tunneling parameter E_{00} is defined as:[9]

$$E_{00} = \frac{qh}{4\pi}\sqrt{\frac{N_a}{m_h \varepsilon_s}}$$

$$= 1.85\times10^{-11}\left[\frac{N_a}{(m_h/m_0)(\varepsilon_s/\varepsilon_0)}\right]$$

$$\approx 1.85\times10^{-11}\left[\frac{N_a}{(A^{**}/120\alpha)(\varepsilon_s/\varepsilon_0)}\right]$$

where the terms have their usual meanings. A^{**} is the effective Richardson constant and α is a fitting parameter which can be found from Norde plots obtained from I-V-T measurements. N_a for the GaN/$Al_{0.2}Ga_{0.8}$N SL layer is 4×10^{18} cm^{-3} at room temperature from Hall measurements.[2] Our study of Ni and Re Schottky barriers on GaN and $Al_xGa_{1-x}N$ indicate that A^{**} can be as small as only 1% of the theoretical value,[10] therefore α is far smaller than 1. Putting these values into the above equation and we can see that $E_{00}/kT>>1$, which satisfies the criteria for a field emission dominated transport regime.

For a tunneling contact, the specific contact resistance $R_c \propto \exp\left(\phi_B/\sqrt{N_a}\right)$. Based on the Schottky-Mott model of metal-semiconductor contacts, the metal-semiconductor

barrier height ϕ_B is related to the work function of the metal ϕ_m and the electron affinity of a *p*-type semiconductor χ_s by $\phi_b = (\chi_s + E_g) - \phi_m$. Therefore, metals with high work functions are expected to give smaller R_c values, which is consistent with the results shown in Figure 2. Pt, with a ϕ_m of 5.65 eV, has the highest work function of all metals and is chemically stable up to 700 °C on GaN.[8] However, experiments have shown that Pt suffers from poor adhesion on GaN and therefore, a thin Ti layer is used to improve adhesion as well as getter surface oxides. The excellent ohmic contacts obtained in this study for Ti/Pt/Au shows that Ti has been quite effective in these roles.

The semiconductor sheet resistance (R_s) obtained from a TLM test has contributions from the reacted layer underneath the metal contact as well as from the bulk semiconductor. Auger electron spectroscopy shows that the reacted layer is less than 20 nm thick for the Ti/Pt/Au contact. In a shallow contact, the measured sheet resistance is very similar to that of the bulk material prior to metal deposition and exhibits similar temperature dependence. The log (R_s) vs. 1000/T plot shown in Figure 4 clearly demonstrates this. Arrhenius activation energies can be extracted from the slopes of the lines shown in Figure 4. Ni/Au contacts did not exhibit linear characteristics on GaN/$Al_{0.1}Ga_{0.9}$N SL and is omitted from the plot. It is seen that the slopes for Pd/Au and Ti/Pt/Au on GaN/$Al_{0.1}Ga_{0.9}$N SL are similar, which are calculated to be about 90 meV. The activation energies obtained from the three metallizations on GaN/$Al_{0.2}Ga_{0.8}$N SL are also similar, and cluster around 60 meV. Both of these values agree very well with the results obtained from conductivity measurements using variable temperature Hall analysis.[2,3] In contrast, the activation energy for Mg acceptors in p-GaN is about 200 meV.[2]

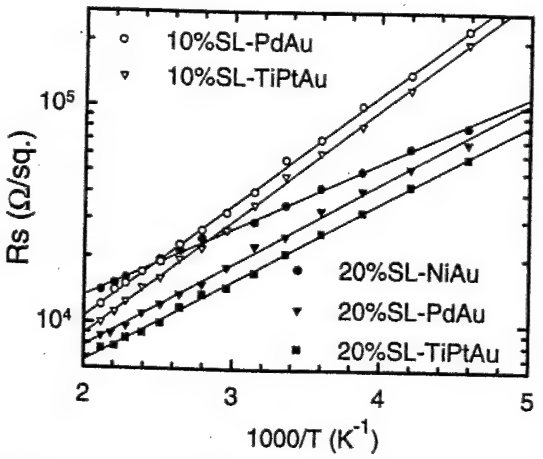

Fig. 4 Dependence of sheet resistance on temperature exhibited by different contacts on GaN/Al_xGa_{1-x}N-SL after annealing. The surfaces were ultrasonically cleaned with BOE prior to photoresist patterning, except for Ti/Pt/Au.

3. Conclusion

We have studied a number of metallization schemes on GaN/Al_xGa_{1-x}N short period superlattices. Ti/Pt/Au metallization compares favorably to other schemes investigated in this study. In addition, low resistivity can be obtained for the Ti/Pt/Au contacts without a prolonged ultrasonic cleaning in BOE, which is required for other bilayer metallizations to achieve good contacts. Temperature-dependent TLM study shows that the current transport is dominated by field emission, which benefited from lowered dopant activation energies for the SL compared to p-GaN. Temperature stability study is still on going. Preliminary results indicate degradation of all "two-step" treated contacts at temperatures above 550 °C while Ti/Pt/Au contacts degraded after annealing at above 500 °C.

Acknowledgments

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Long-term thermal stability of Ti/Al/Mo/Au ohmic contacts on n-GaN

D. Selvanathan, L. Zhou, V. Kumar, and I. Adesida

Department of Electrical and Computer Engineering and Micro and Nanotechnology Laboratory,

University of Illinois at Urbana Champaign, Urbana, IL – 61801, USA

and

N. Finnegan

Materials Research Laboratory,

University of Illinois at Urbana Champaign, Urbana, IL – 61801, USA

ABSTRACT

Improved performance of the ohmic contacts on n-GaN has been demonstrated with the use of MoAu as the capping layer on TiAl metallization. Contact resistance as low as 0.13 Ω-mm was achieved in these ohmic contacts when annealed at 850 °C for 30 s. We have studied the long-term thermal stability of these contacts at 500 °C, 600 °C, 750 °C and 850 °C, respectively. Ti/Al/Mo/Au metallization forms low-contact resistance ohmic contacts on n-GaN that are stable at 500 °C and 600 °C after 25 h of thermal treatment. The ohmic contact performance degrades after 10 h of thermal treatment at 750 °C while the contacts exhibit non-linear current-voltage characteristics after 1 h of thermal treatment at 850 °C, with the formation of oxide on the surface of the contacts accompanied by surface discoloration. The intermetallic reactions taking place in the contacts during the long-term thermal treatments were studied using Auger electron spectroscopy and the surface morphology was characterized using atomic force microscopy.

INTRODUCTION

GaN-based materials are direct wide-band-gap semiconductors that have found many device applications. Such applications include opto-electronic devices such as photo-detectors, blue/ultraviolet laser diodes, light emitting diodes, metal-semiconductor field effect transistors (MESFETs), and high electron mobility transistors (HEMTs).[1-6] MESFETs and HEMTs are important for high power and high temperature electronics. These devices require low resistance, thermally stable ohmic contacts to operate efficiently at high temperature and high frequency. Many metallization schemes have been proposed for ohmic contacts on n-GaN.[7-12] Among these, Ti/Al has become the metallization scheme of choice to achieve low resistance ohmic contacts on n-GaN. Since the Ti and Al layers are easily prone to oxidation, ohmic contact resistance degrades with prolonged exposure to ambient atmosphere and also during annealing at elevated temperatures. Ti/Au, Pt/Au, Ni/Au have been used as capping layers to prevent the oxidation of the underlying metal layers.[13-15] Recently, we have reported the use of Mo/Au as the capping layer on Ti/Al ohmic metallization to achieve low resistance, thermally stable ohmic contacts on n-GaN.[16] The use of Mo/Au prevented the oxidation and lateral flow of Ti/Al layers when the contacts were annealed at high temperatures. Also, smooth surface morphology was achieved in these ohmic contacts. Ti/Al/Mo/Au ohmic contacts were stable after thermally aging these contacts at 500 °C for 350 h in a furnace. In this paper, we present more details on the long-term thermal stability of Ti/Al/Mo/Au ohmic contacts on n-GaN at high temperatures and study the electrical properties of these contacts after long-term thermal treatment using linear transfer length measurements (TLM). The interactions between the various metal layers and the GaN

epilayer during annealing were investigated by depth profiling using Auger electron spectroscopy (AES) and the surface morphology was characterized using atomic force microscopy (AFM).

EXPERIMENTAL PROCEDURE

The epitaxial GaN layer used in this work was grown on a sapphire substrate using metalorganic-chemical vapor deposition. A 1 μm-thick undoped semi-insulating GaN on an AlN buffer layer was grown on the sapphire substrate followed by 1 μm-thick, Si doped n-GaN layer. From Hall measurements, the bulk carrier concentration was measured to be 1×10^{18} cm^{-3} and the mobility was ~ 250 $cm^2/V\text{-}s$. The layers were degreased and sonicated in acetone and iso-propyl alcohol and blow-dried using N_2 to remove the organic contaminants on the surface. Mesas were etched using Cl_2/Ar plasma in an inductively-coupled-plasma reactive ion etch (ICP-RIE) system to electrically isolate the various TLM structures. Next the ohmic contact pads were patterned using optical lithography. Prior to metallization the surfaces were treated using $SiCl_4$ plasma in reactive ion etching (RIE) system with a $SiCl_4$ flow rate of 10 sccm and a plasma self-bias voltage of –300 V, and followed by a buffered oxide etch (BOE) and DI water rinse to remove any surface oxide.[17] Thereafter, an ohmic metallization consisting of Ti (15 nm) /Al (65 nm) / Mo (X nm) / Au (50 nm) was deposited. To study the effect of thickness of Mo on the electrical performance of these contacts, three different samples were prepared with the thickness (X) of the Mo layer being 25 nm, 35 nm and 50 nm, respectively. Ti, Al and Mo were electron-beam evaporated while Au was thermally evaporated. The TLM ohmic pads were delineated using a lift-off process and the gap spacings between the TLM contacts were 2, 3, 4, 5, 6, 8, and 10 μm, respectively. The

contacts were alloyed at several temperatures ranging from 750 °C to 900 °C for 30 s in N_2 ambient in a rapid thermal annealing (RTA) furnace. Current-voltage (I-V) measurements were made at room temperature using an HP4142B semiconductor analyzer. AES spectra were taken using a Physical Electronics Incorporated 660 Scanning Auger Multiprobe with a 5 keV primary electron beam, incident at an angle of 30° to the surface normal and the spot size of the e-beam was 0.3 μm. The samples were sputtered with a 750 eV, 34 $\mu A/cm^2$ Ar ion beam and the AES spectra were analyzed using PEI Multipak software ver. 6.0. The depth profiles were obtained by monitoring the distributions of the various elements in the contacts such as Ti (421 eV), Al (1396 eV), Mo (2044 eV), Au (2022 eV), Ga (1069 eV), N (389 eV), O (510 eV) and C (275 eV). The peak electron energies monitored are given in parenthesis. The AFM measurements were performed with a Digital Instruments 3000 scanning atomic force microscope and the micrographs were analyzed using Nanoscope Vision software ver. 4.0. The root mean-square (RMS) value for surface roughness of these contacts was measured from analysis of a 5×5 μm^2 area on the sample. The annealed contacts were placed in a furnace with N_2 gas flow to study the long-term thermal stability of these contacts. The samples were not sealed in evacuated ampoules when thermally treated in the furnace.

EXPERIMENTAL RESULTS AND DISCUSSION

The ohmic performance of the Ti/Al/Mo/Au contacts on n-GaN was characterized by measuring the contact resistance and specific contact resistivity using I-V measurements method. Figure 1 shows the I-V responses measured on the TLM pads with a gap spacing of 5 μm. The I-V curves are plotted as a function of the anneal

temperature varying from 750 °C to 900 °C. The I-V response of the as-deposited ohmic contacts is shown in the inset. The as-deposited ohmic contacts displayed non-linear I-V response while the annealed contacts are ohmic. The resistance of the ohmic contacts decreased as the anneal temperature increased from 750 °C to 900 °C with the contacts annealed at 850 °C exhibiting the minimum resistance. The contact resistance is extracted from a linear curve fit of the measured resistance vs gap spacing plot. The y-intercept ($2R_c$) and the slope determine contact resistance (R_c) and sheet resistance (R_s), respectively. The value for specific contact resistivity (ρ_c) is calculated from R_c and the x-intercept. The contact resistance and specific contact resistivity of the ohmic contacts on n-GaN were measured as a function of the anneal temperature and the results averaged over several TLM structures are summarized in Fig. 2. The contact resistance (specific contact resistivity) of the ohmic contacts with a Mo thickness of 25 nm varied from 0.24 Ω-mm (6×10^{-6} Ω-cm^2) at an anneal temperature of 750 °C to a minimum of 0.13 Ω-mm (1.5×10^{-6} Ω-cm^2) at an anneal temperature of 850 °C, and thereafter, the contact resistance increased as the anneal temperature was increased. Contacts with a Mo thickness of 35 nm exhibited a variation in the contact resistance from 0.20 Ω-mm (4×10^{-6} Ω-cm^2) when annealed at 750 °C to a minimum contact resistance of 0.17 Ω-mm (2.4×10^{-6} Ω-cm^2) when the contacts were annealed at 850 °C. The contacts with a Mo thickness of 50 nm exhibited a minimum value of contact resistance of 0.16 Ω-mm (2.3×10^{-6} Ω-cm^2) when annealed at 750 °C. The specific contact resistivity of these ohmic contacts exhibits a similar trend as a function of the Mo thickness. The contact resistance of these ohmic contacts is more or less constant when varying the anneal

temperature from 750 °C to 900 °C. Thus there is no significant dependence in the performance of these ohmic contacts on the thickness of the Mo layer.

Ohmic contacts with a Mo thickness of 25 nm annealed at 850 °C for 30 s were used to investigate the performance of these contacts during long-term thermal aging process. Long-term thermal stability experiments were performed by treating the annealed ohmic contacts at 500 °C, 600 °C, 750 °C and 850 °C, respectively for 25 hours. The contact resistance of the ohmic contacts was measured at various intervals of time and the results are plotted in Fig. 3. From the results, we can infer that that the Ti/Al/Mo/Au ohmic contacts are thermally stable up to 600 °C even after 25 hours of thermal treatment. The contact resistance does not change significantly (< 10%) during the long-term thermal aging process at 500 °C and 600 °C. When the contacts were heated at 750 °C, the contact resistance degraded rapidly after 10 hours of thermal treatment and when the temperature was increased to 850 °C, the ohmic contacts degraded after 1 hour of thermal treatment. The contacts exhibited a non-linear I-V response when they were degraded and hence the contact resistance was not measured in this case.

Figure 4 shows the AES depth profile of as-deposited Ti/Al/Mo/Au ohmic contacts on n-GaN. Ti, Al, Mo, Au layers are clearly demarcated on the GaN substrate in the spectra. The N layer is seen to encompass the Ti peak suggesting the formation of a Ti-N compound at the GaN interface even before annealing the contacts. This is consistent with the previously published reports on Ti/Al ohmic contact on n-GaN studied using transmission electron microscopy (TEM) measurements.[18] There is a trace of O in the Mo layer indicating that the source may have gettered oxygen resulting in trace amounts of Mo-O compound. The AES depth profile of the Ti/Al/Mo/Au ohmic

contacts annealed at 850 °C for 30 s is shown in Fig. 5 and it is seen that there is significant intermixing between the various metals. Al is uniformly distributed in the contact and Ti has out-diffused to the surface of the contact. Au and Mo have moved towards the GaN interface but haven't diffused into the GaN layer. N has out diffused from the substrate to the surface of the contact. The O level on the surface is increased when compared to the as-deposited sample indicating the formation of an oxide on the surface of the ohmic contact during the annealing process.

Figure 6 shows the AES depth profile for the contacts annealed at 850 °C for 30 s and then thermally treated at 500 °C for 10 h. O and Ti depth profiles are similar to those shown in Fig. 5. Mo and Au layers are seen to penetrate further into the Ga-N interface. Since the metals in the ohmic contact have diffused into the GaN epilayers, Ga is present after 30 minutes of depth profiling when compared to the annealed contact where in Ga is present after 40 minutes of sputtering. Al layer thickness is a maximum at the surface and decreases as we go towards the Ga-N interface. The O layer is found to mimic the Al depth profile and thus the oxide layer can be deduced to be an Al-O compound. The ohmic contacts exhibit a linear I-V response when annealed at 500 °C for 10 h in spite of the in-diffusion of Au and Mo layers and the increase in the surface oxide as indicated by the AES depth profiles.

Figure 7 shows the AES depth profile for the contacts annealed at 850 °C for 30 s and then thermally treated at 850 °C for 5 h. From Fig. 3, it is seen that the ohmic contacts have degraded after 2 h of long-term thermal treatment of the annealed ohmic contacts at 850 °C. Figure 7 is the AES depth profile of a degraded ohmic contact, which shows a non-linear I-V response. From the figure, we observe significant increase

in the surface oxide compared to the previous AES depth profiles. Also the O and Al layers exhibit a similar trend thereby indicating that the oxide formed is an Al-O compound. The increase in oxide layer in the ohmic contact can be attributed to the O_2 presence in ambient in the heating furnace, in spite of the N_2 flow. Mo and Au layers have penetrated deep into the Ga-N interface while Ti layer is similar to that found in the previous AES depth profiles. Ga layer is detected after 30 minutes of sputtering as seen in the AES depth profile of the annealed ohmic contact thermally treated at 500 °C for 10 h. N is present throughout the contact indicating the out-diffusion of N. Thus when the contacts have degraded, the Au and Mo layers are diffused deep into the GaN layer and there is significant presence of oxide in the ohmic contacts.

The AFM scans of the surface of the un-annealed ohmic contacts and the contacts annealed at 850 °C are shown in Fig. 8 and Fig. 9. The RMS values for surface roughness for the un-annealed and annealed contacts are measured to be 3 nm and 26 nm, respectively. After long-term thermal treatment at 850 °C for 5 h, the RMS value for surface roughness increased to 44 nm. Micrographs of the ohmic contact surface prior to annealing and after annealing at 850 °C for 30 s and after long-term thermal treatment at 500 °C for 10 h and at 850 °C for 5 h are shown in Figs 10(a), 10(b), 10(c) and 10(d), respectively. The un-annealed contact surface is smooth while the annealed ohmic contacts are seen to have rough textured surfaces. The contact surface color changed from a dark gold color in the un-annealed contacts to a light tan color in the annealed contacts and to a dark tan color in the contacts thermally treated at 500 °C for 10 h and to golden bluish green color when the contacts were thermally treated at 850 °C for 5 h. This discoloration is indicative of oxide formation on the surface of the contacts and the

ohmic performance of the contacts degraded, exhibiting a non-linear I-V response in this case. The metal contacts also became brittle and peeled away when probed for I-V characteristics.

SUMMARY

Improved performance of the ohmic contacts has been demonstrated with the use of MoAu as the capping layer on TiAl metallization. Contact resistance as low as 0.13 Ω-mm was achieved in these ohmic contacts when annealed at 850 °C for 30 s. Also the long-term thermal stability of these contacts at high temperatures has been studied. Ti/Al/Mo/Au metallization forms low-contact resistance ohmic contacts on n-GaN that are stable at 600 °C after 25 h of thermal treatment. The ohmic contact performance degrades at higher temperature with the formation of oxide on the surface of the contacts and surface discoloration is seen in this case and also the contacts become brittle. There was no significant change in the performance of the ohmic contacts when the thickness of the Mo layer was increased. In Ti/Al/Mo/Au ohmic contacts, the Au and Mo layers penetrate into the GaN epilayer when the annealed ohmic contacts were thermally treated at high temperatures and also there was significant growth of oxide in the ohmic contacts. The degradation of the ohmic contacts when thermally aged at high temperatures can be attributed to the in-diffusion of Au and Mo layers and also to the oxide formation in these contacts. The exact mechanism of ohmic contact formation is not clearly understood and is the subject of interest for future research. The performance of these contacts when thermally treated in evacuated ampoules is to be studied in the future to ascertain whether the oxidation of the contacts or the in-diffusion of metal layers is the cause for the degradation of the ohmic contacts.

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Fig. 1. Current-voltage characteristics of Ti (15 nm)/ Al (60 nm)/ Mo (25 nm)/ Au (50 nm) ohmic contacts on n-GaN as a function of the anneal temperature. The contacts were annealed for 30 s in a N_2 ambient. The non-linear current-voltage response of an un-annealed ohmic contact is shown in the inset.

Fig. 2. Contact resistance and specific contact resistivity of Ti (15 nm)/Al (60 nm)/Mo (X) /Au (50 nm) ohmic contacts on n-GaN annealed for 30 s, as a function of the anneal temperature. The thickness (X) of Mo was varied from 25 nm to 50 nm. The filled symbols represent the contact resistance and the clear symbols represent the specific contact resistivity.

Fig. 3. Long-term thermal treatment characteristics of Ti/Al/Mo/Au ohmic contacts on n-GaN using contact resistance as a measure of the ohmic performance of the contacts.

Fig. 4. Auger electron spectroscopy (AES) depth profile of the un-annealed Ti/Al/Mo/Au ohmic contact on n-GaN.

Fig. 5. AES depth profile of Ti/Al/Mo/Au ohmic contact on n-GaN annealed at 850 °C for 30 s. The annealed contacts exhibit a linear I-V response.

Fig. 6. AES depth profile of Ti/Al/Mo/Au ohmic contact on n-GaN annealed at 850 °C for 30 s and then thermally treated in a furnace at 500 °C for 10 h. The ohmic contact exhibits a linear I-V response after long-term thermal treatment at 500 °C for 10 h.

Fig. 7. AES depth profile of Ti/Al/Mo/Au ohmic contact on n-GaN annealed at 850 °C for 30 s and then thermally treated in a furnace at 850 °C for 5 h. The performance of the ohmic contact degrades significantly, exhibiting a non-linear I-V response after long-term thermal treatment at 850 °C for 5 h.

Fig. 8. Atomic force micrograph of the un-annealed Ti/Al/Mo/Au ohmic contacts on n-GaN. The RMS value for surface roughness is measured to be 3 nm.

Fig. 9. Atomic force micrograph of the Ti/Al/Mo/Au ohmic contacts on n-GaN annealed at 850 °C for 30 s. The RMS value for surface roughness is measured to be 26 nm.

Fig. 10. Micrographs of the Ti/Al/Mo/Au ohmic contacts on n-GaN. (a) un-annealed ohmic contact surface, (b) ohmic contact annealed at 850 °C for 30 s, (c) annealed contacts thermally aged at 500 °C for 10 h, and (d) annealed contacts thermally aged at 850 °C for 5 h.

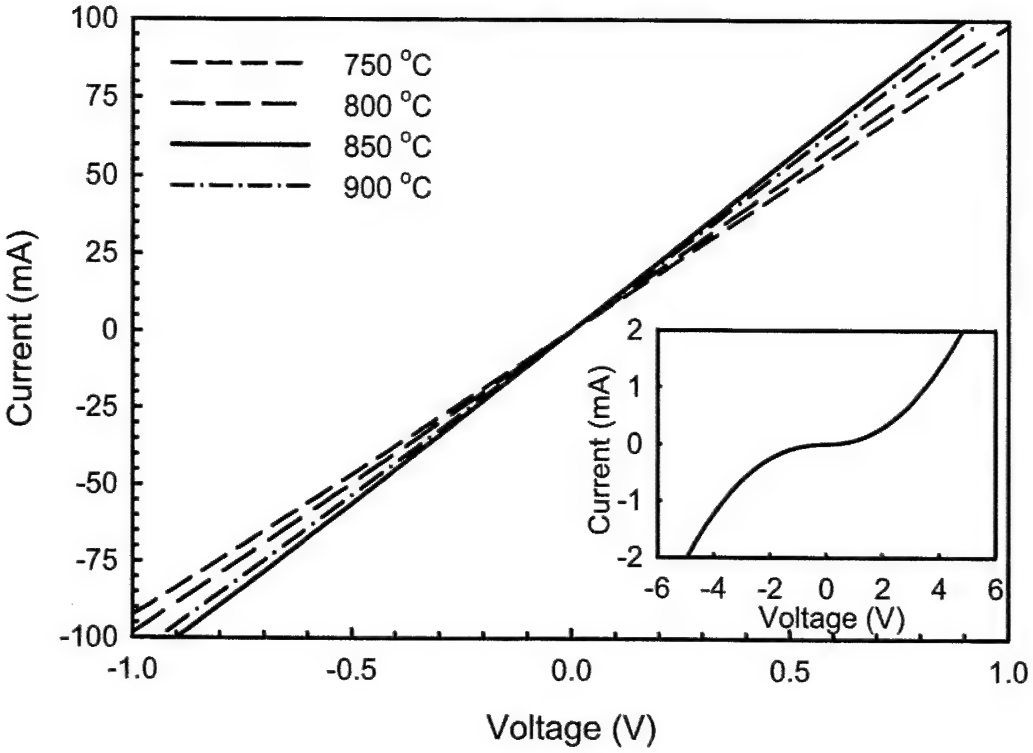

Figure 1

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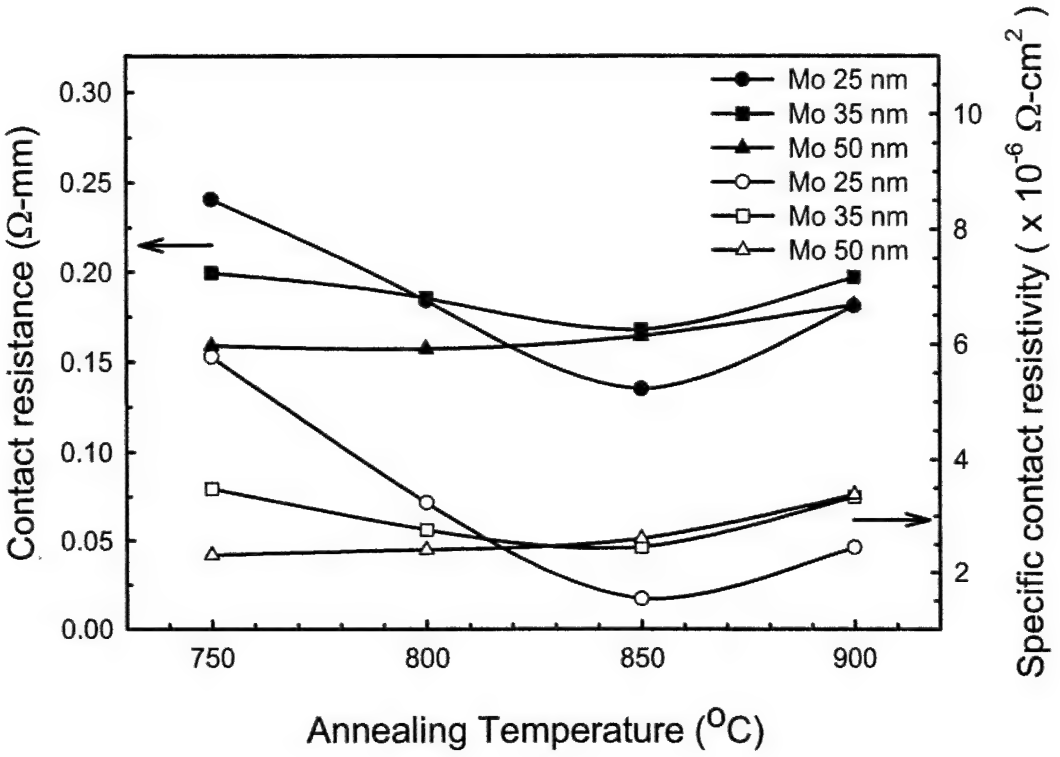

Figure 2

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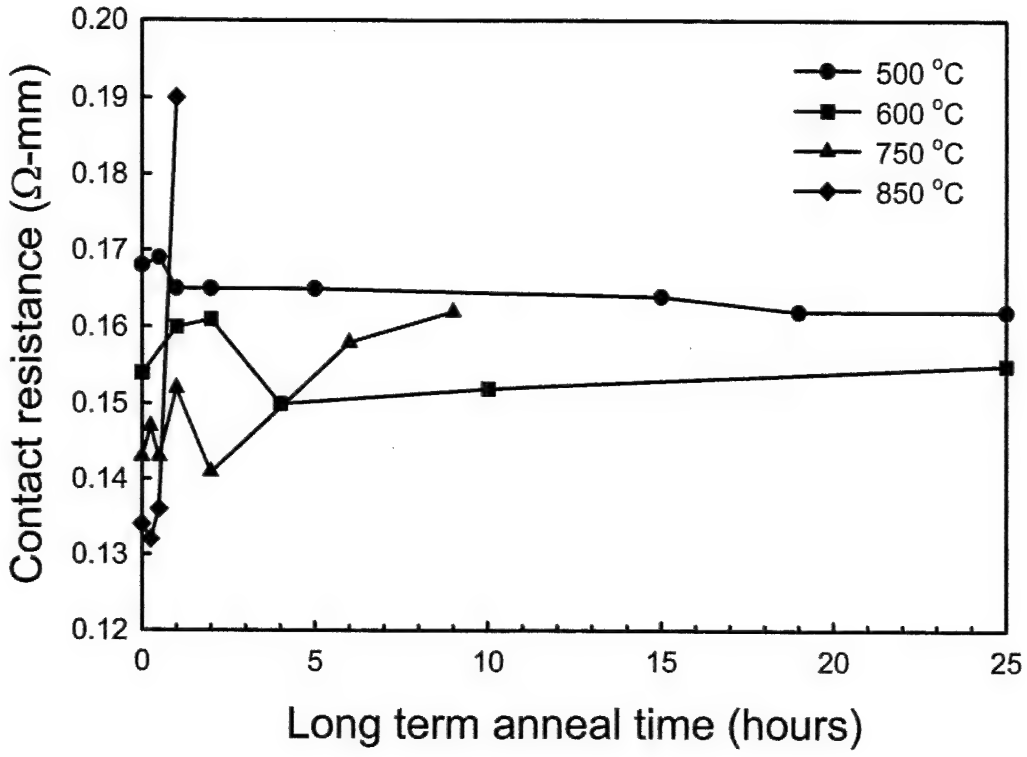

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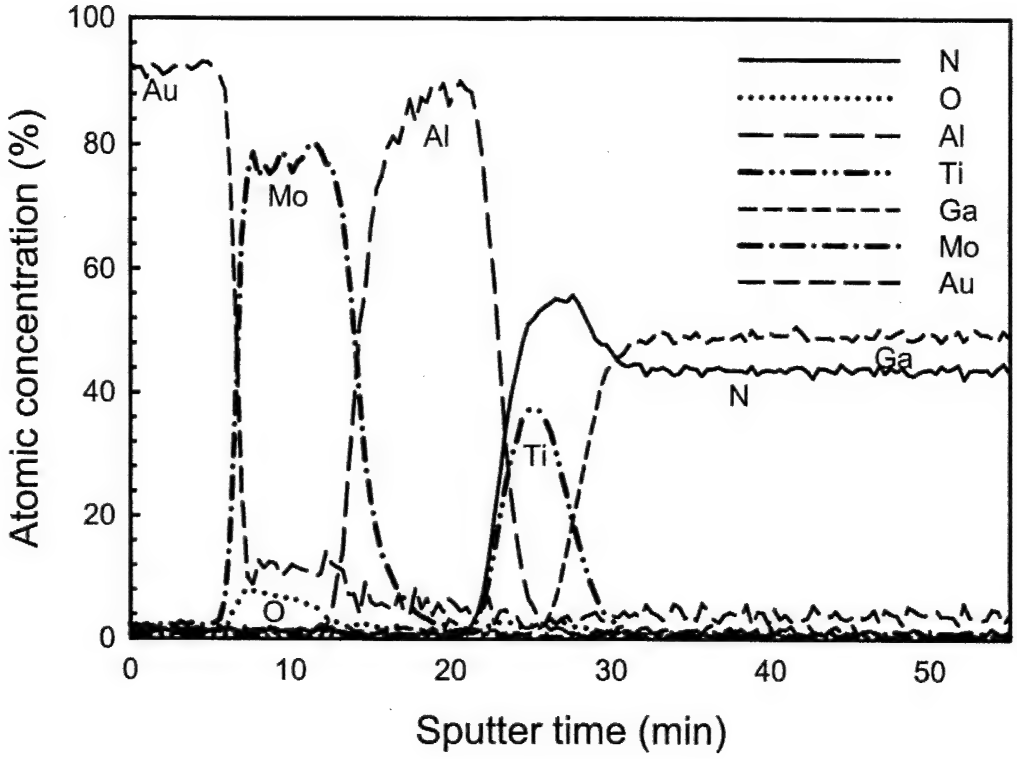

Figure 4

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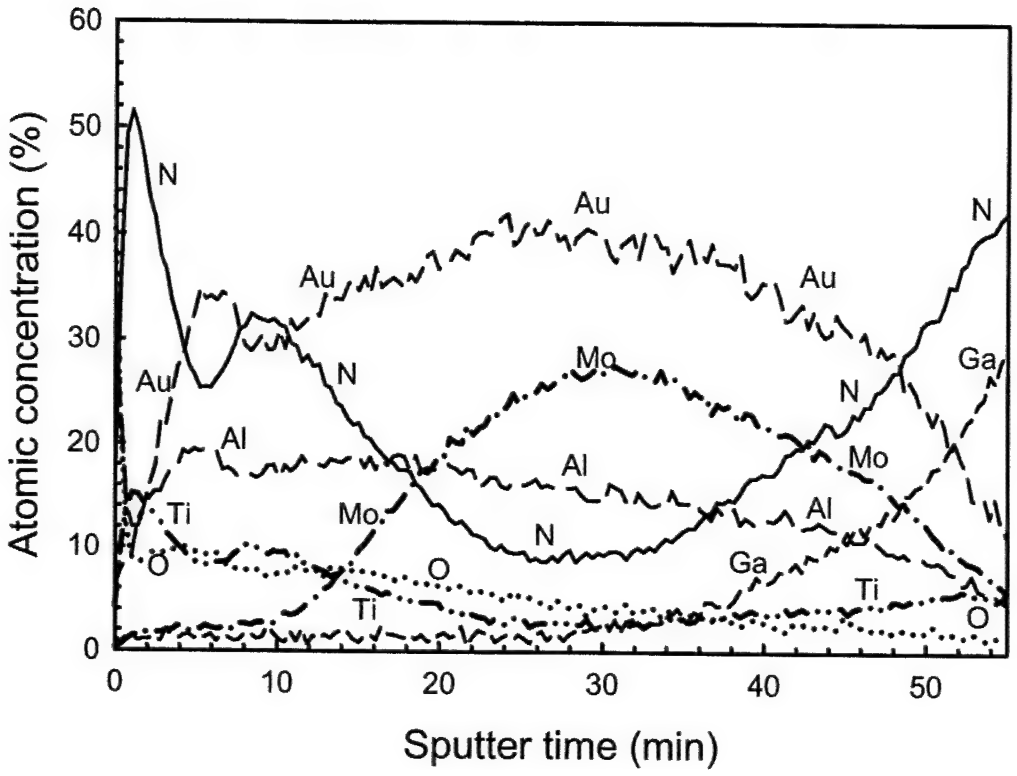

Figure 5

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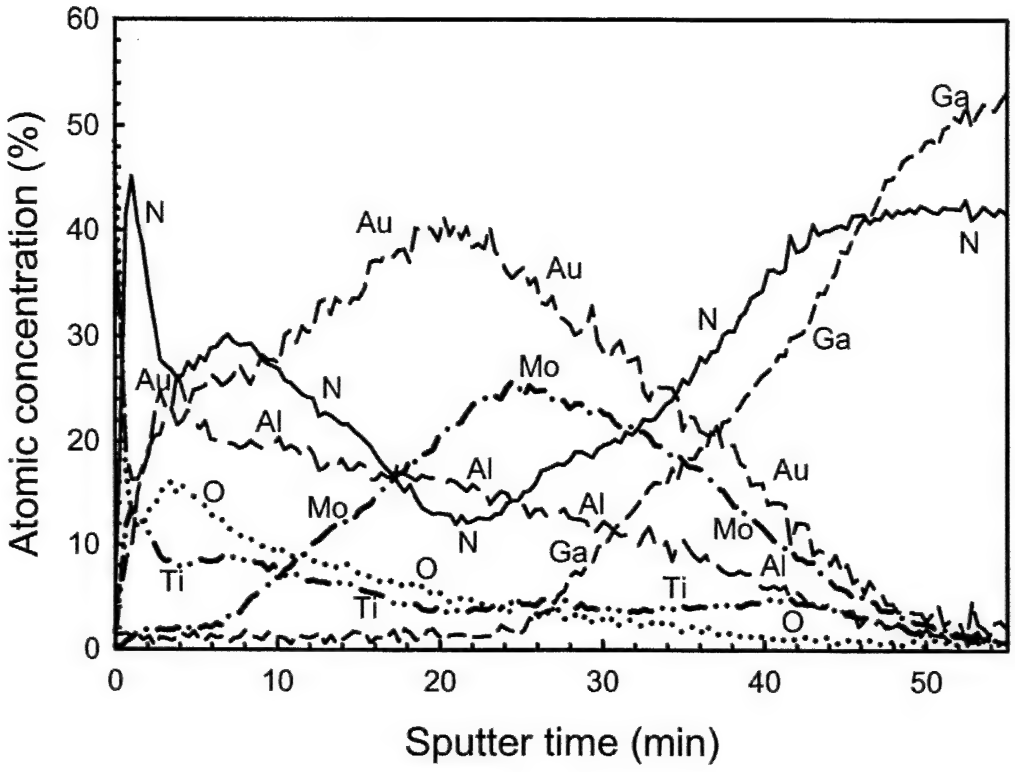

Figure 6

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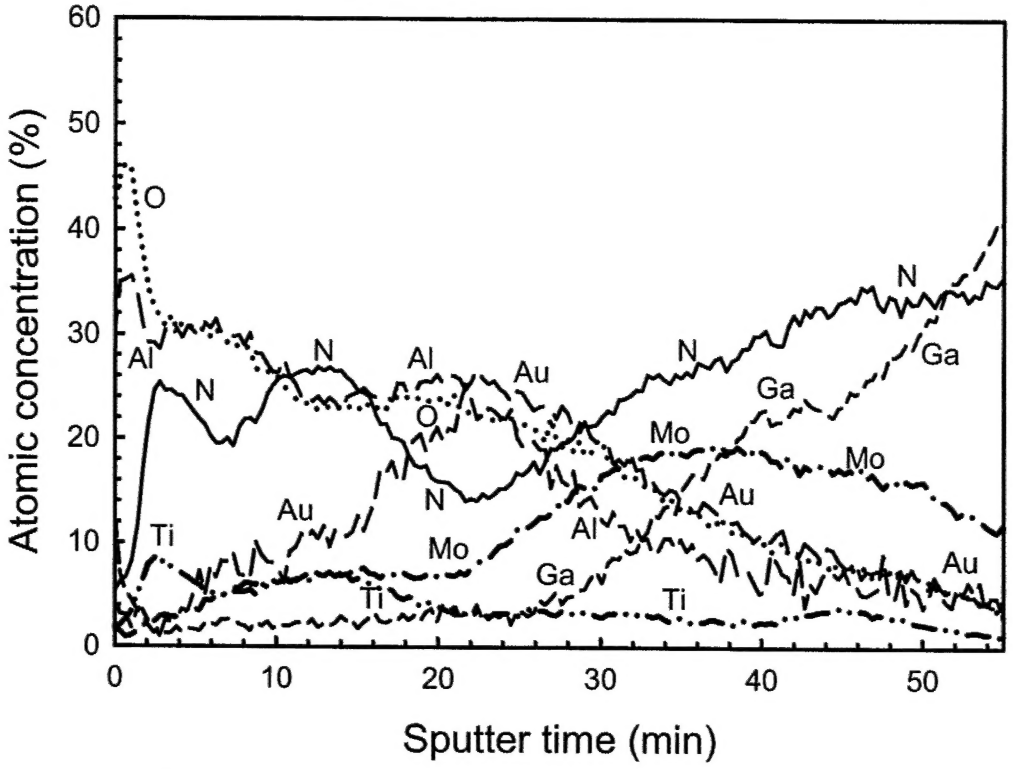

Figure 7

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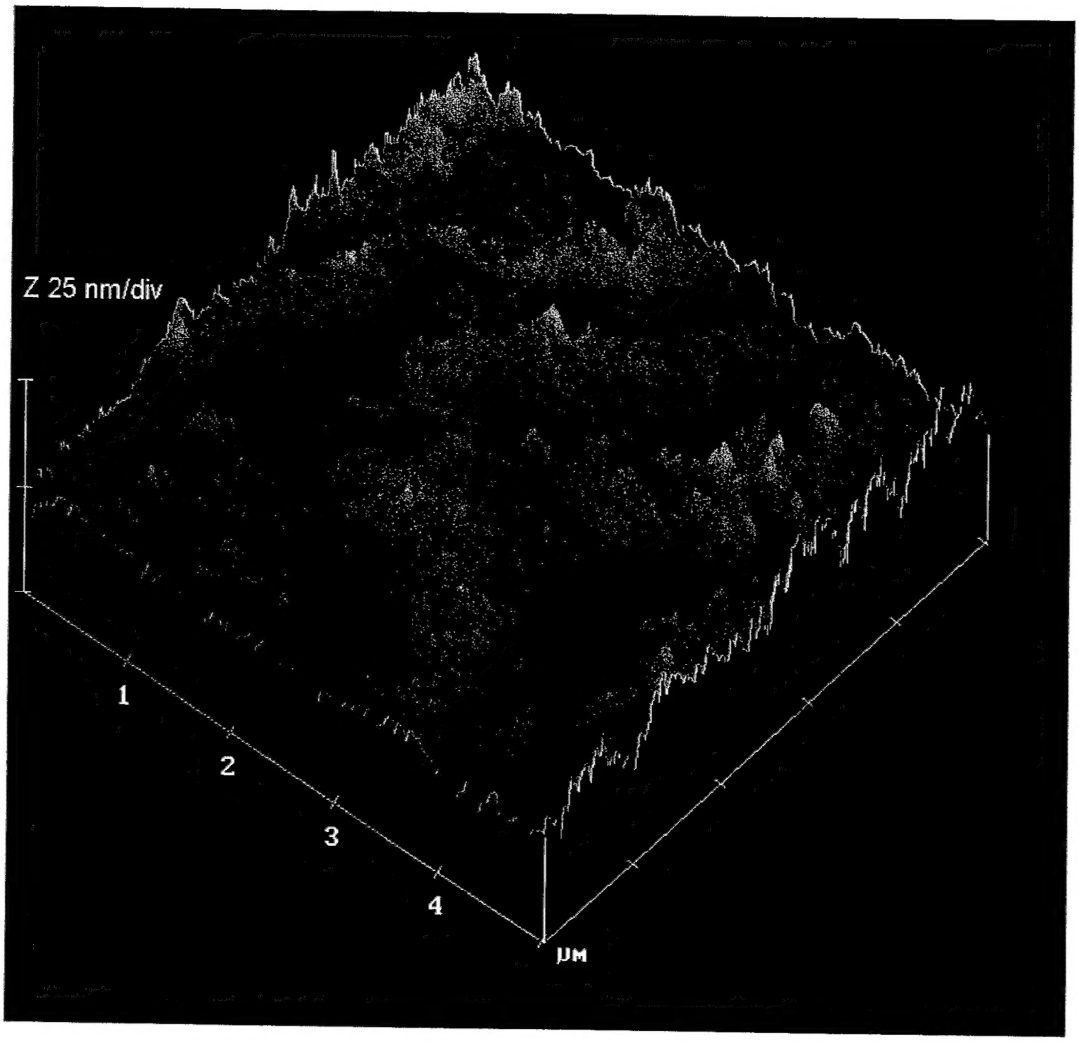

Figure 8

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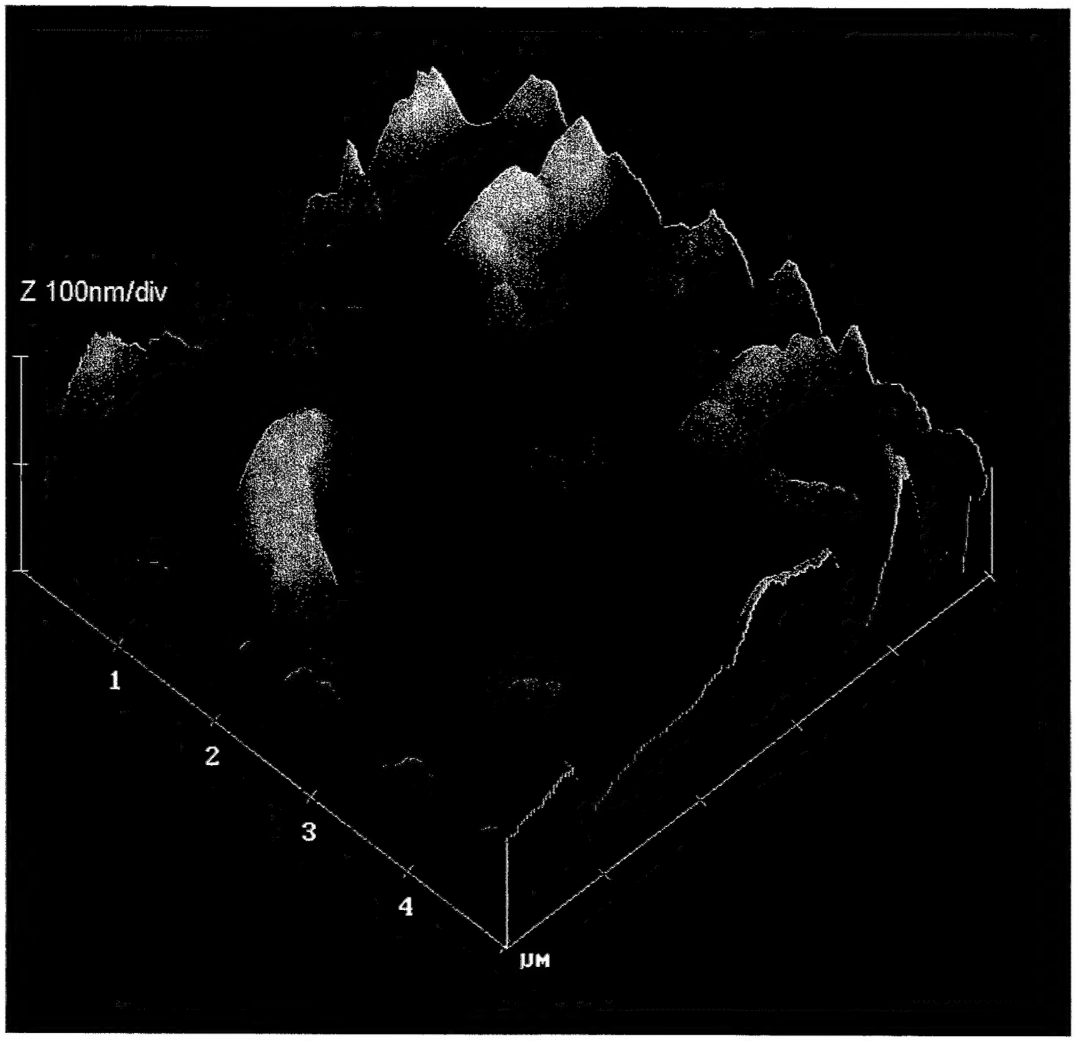

Figure 9

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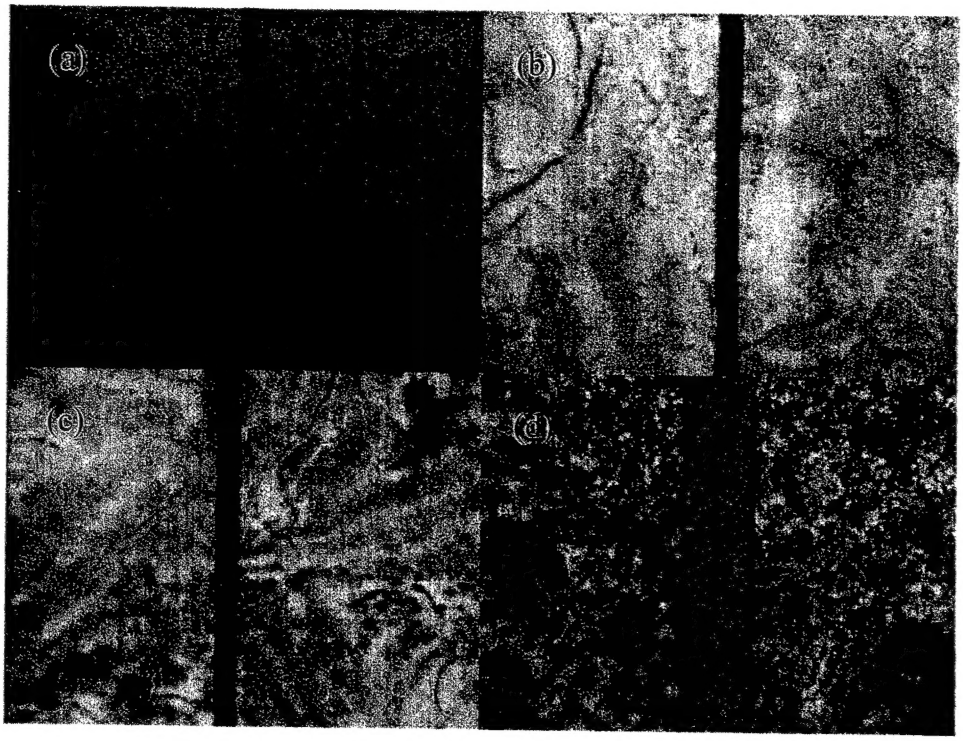

Figure 10

Selvanathan et al.